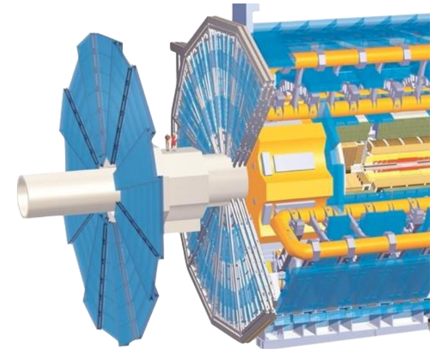


UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

ckhsu@utexas.edu

May 19, 2017

TEXAS
The University of Texas at Austin

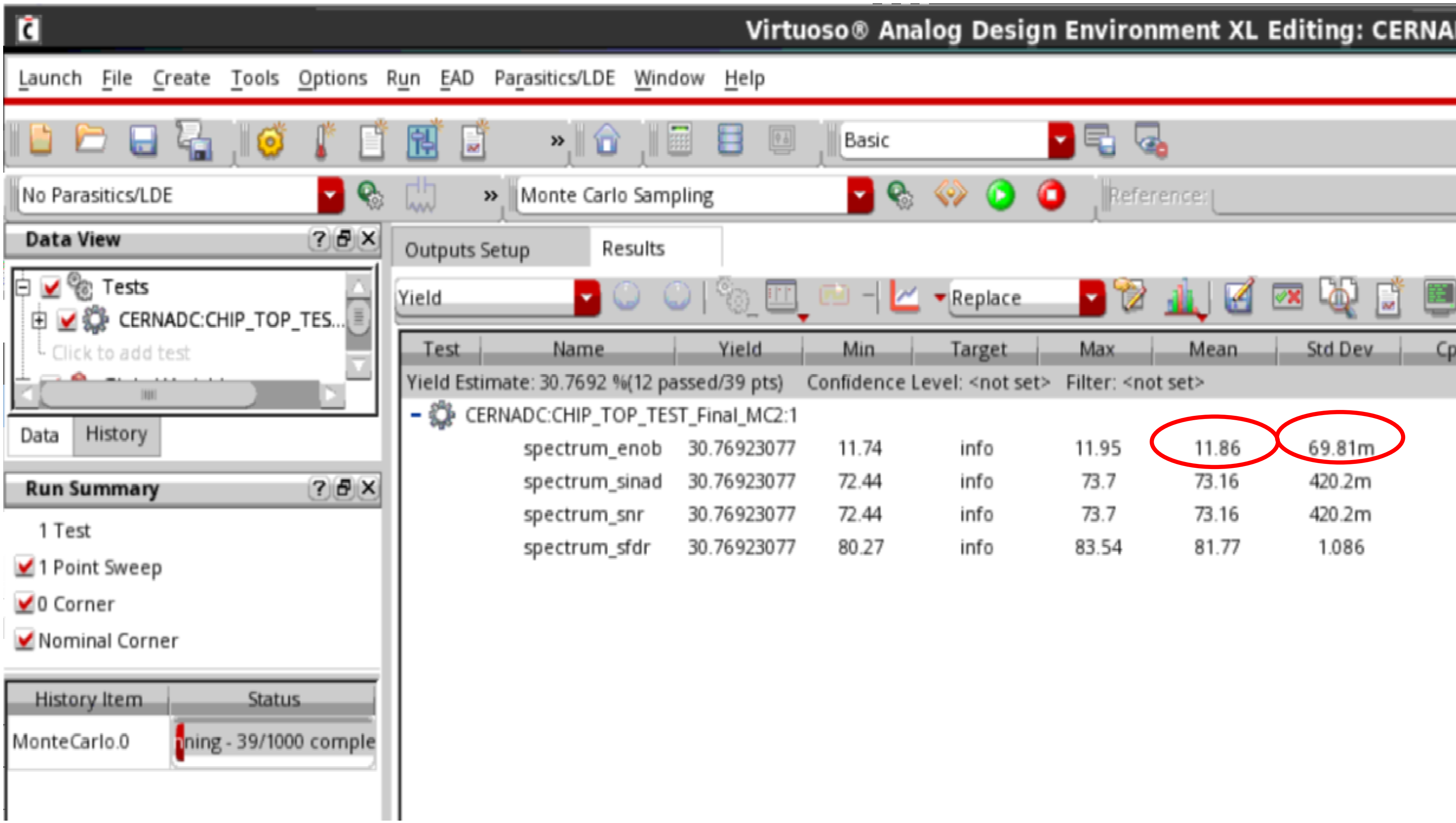
Simulation added

ATLAS EXPERIMENT

Simulation in new verison ADC

Pre-sim Corner(45 corner) with bond wire and noise	Done
Post-sim c+cc for 2nd stage and amp	Done
Post-sim c+cc for 1st stage	Done
Post-sim c+cc for with whole chip	Done
Post-sim corner (45 corner)	Done
Monte Carlo(Pre-sim)	Still Running
Monte Carlo(Post-sim)	After Pre-sim

Monte Carlo Simulation

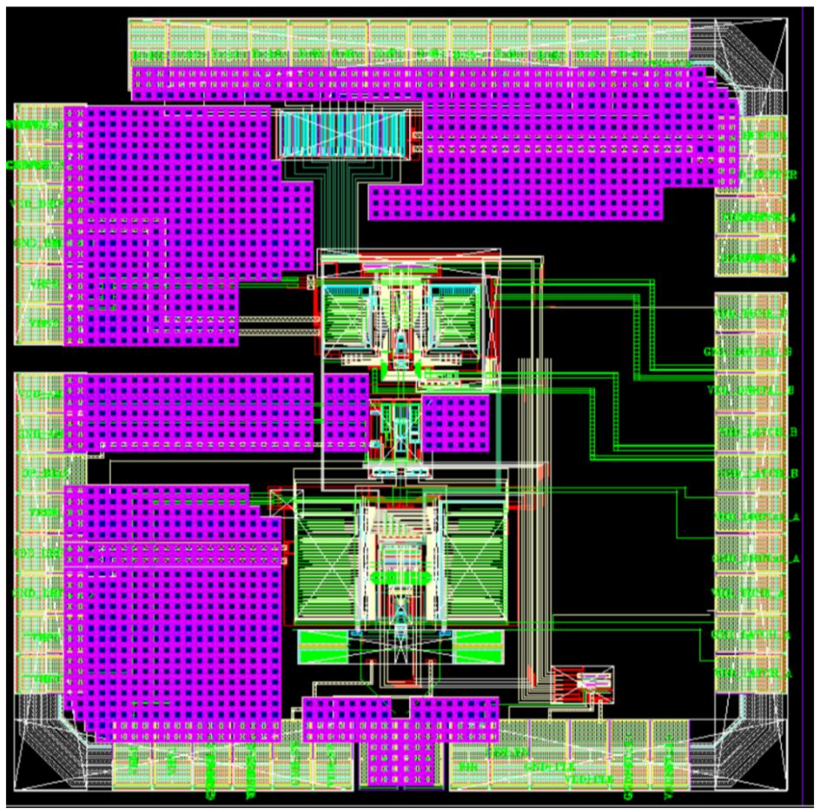


Layout status- Product ADC

- **Finish integration routing. And LVS is clean now.**
- **The unfinished thing for this product adc is putting some bypass capacitor on power path.**

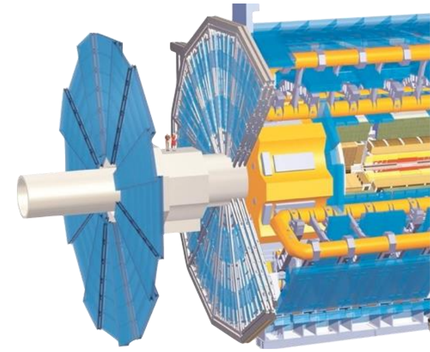
Layout status- Research ADC

- **LVS is clean also.**
- **Bypass capacitor is almost done. Few power path are still need to connected. Finish by this afternoon.**



Future

- Currently, ray is helping me on putting bypass on product adc.
- After I finish Research ADC, I will start to do that with Ray.



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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May 11, 2017

Review

Parameter	C0_2	C0_2	C0_2	C0_2	C0_0	C0_1	C0_2
Model Group	TT	FF	FS	SF	SS	SS	SS
VDD	1.08	1.08	1.08	1.08	1.08	1.08	1.08
temperature	80	80	80	80	-20	27	80
Output	**C0_2**	**C0_2**	**C0_2**	**C0_2**	**C0_0**	**C0_1**	**C0_2**
/DOUT							
spectrum_enob	10.71	10.21	10.06	10.49	9.541	10.11	9.719
spectrum_sinad	66.25	63.2	62.31	64.94	59.2	62.63	60.27
spectrum_snr	66.25	63.2	62.31	64.94	59.2	62.63	60.27
spectrum_sfdr	73.69	69.48	69.49	71	66.23	68.6	67.14

- While operating at 5 corners shown above, ADC can not meet our spec.

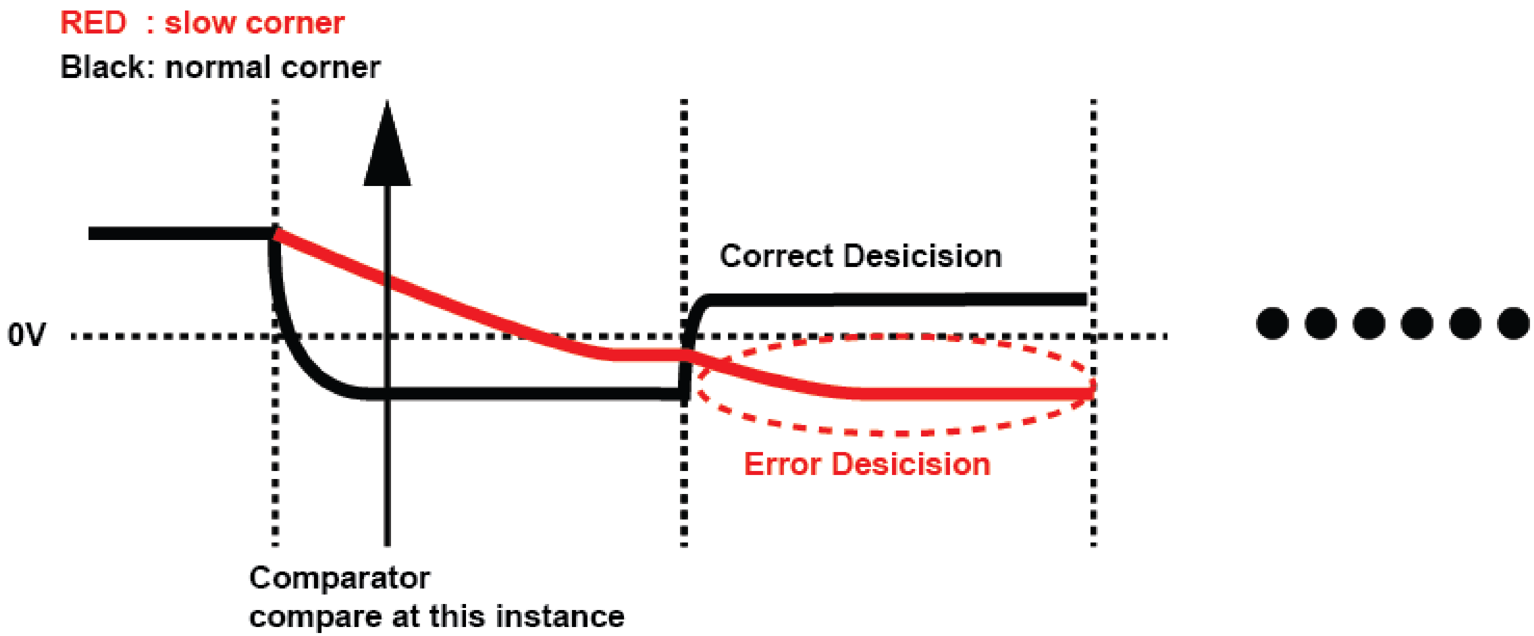
After correction

Parameter	C0_2	C0_2	C0_2	C0_2	C0_0	C0_1	C0_2
Model Group	TT	FF	FS	SF	SS	SS	SS
VDD	1.08	1.08	1.08	1.08	1.08	1.08	1.08
temperature	80	80	80	80	-20	27	80
Output	**C0_2**	**C0_2**	**C0_2**	**C0_2**	**C0_0**	**C0_1**	**C0_2**
/DOUT							
spectrum_enob	10.71	10.21	10.06	10.49	9.541	10.11	9.719
spectrum_sinad	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
spectrum_snr	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
spectrum_sfdr	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

11.04 11.12 11 .02 11.14 10.8 11.01 11.21

Problems in 0.9VDD

- DAC settling becomes very slow in low voltage, leading to error decision.



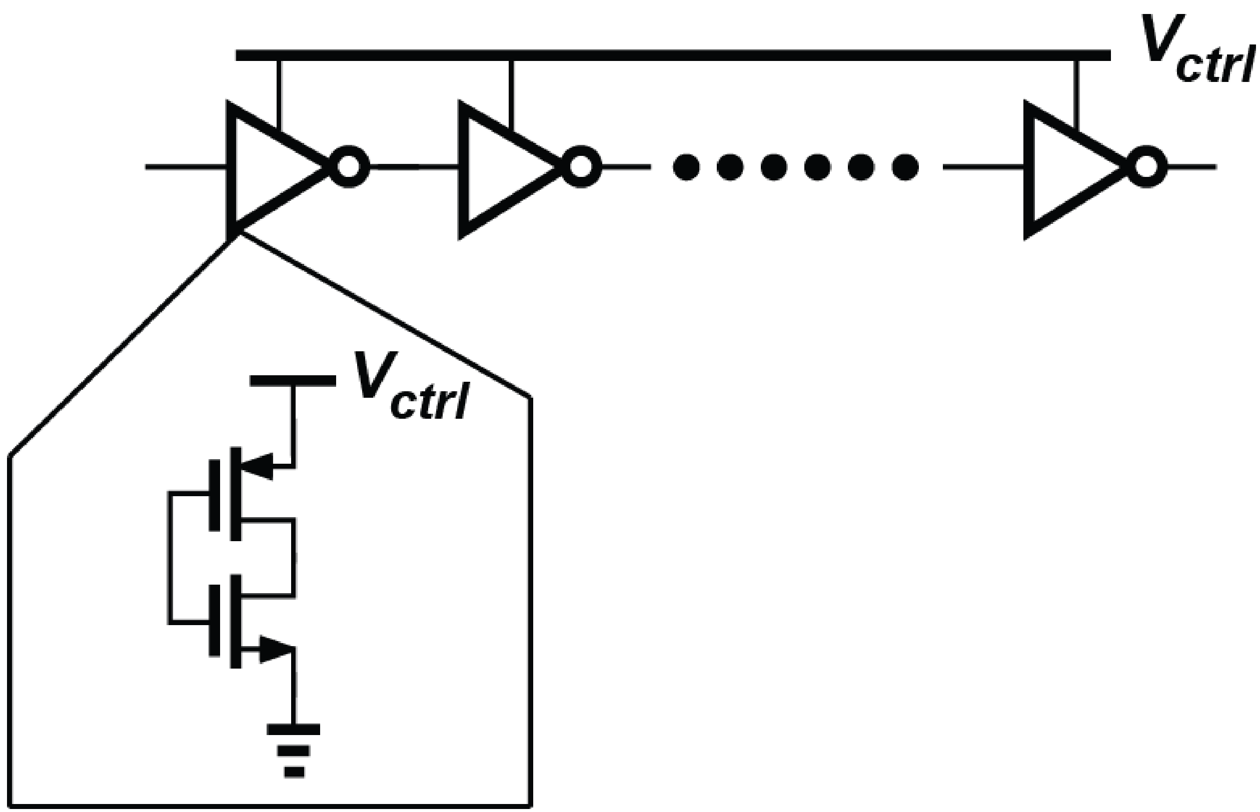
Correction method

- **1. Adding some delay to delay a signal which activate a comparator.**

- **2. Implement redundancy to second stage.**
  (Hasn't been implemented in first tapeout. Will be implemented in next verison)

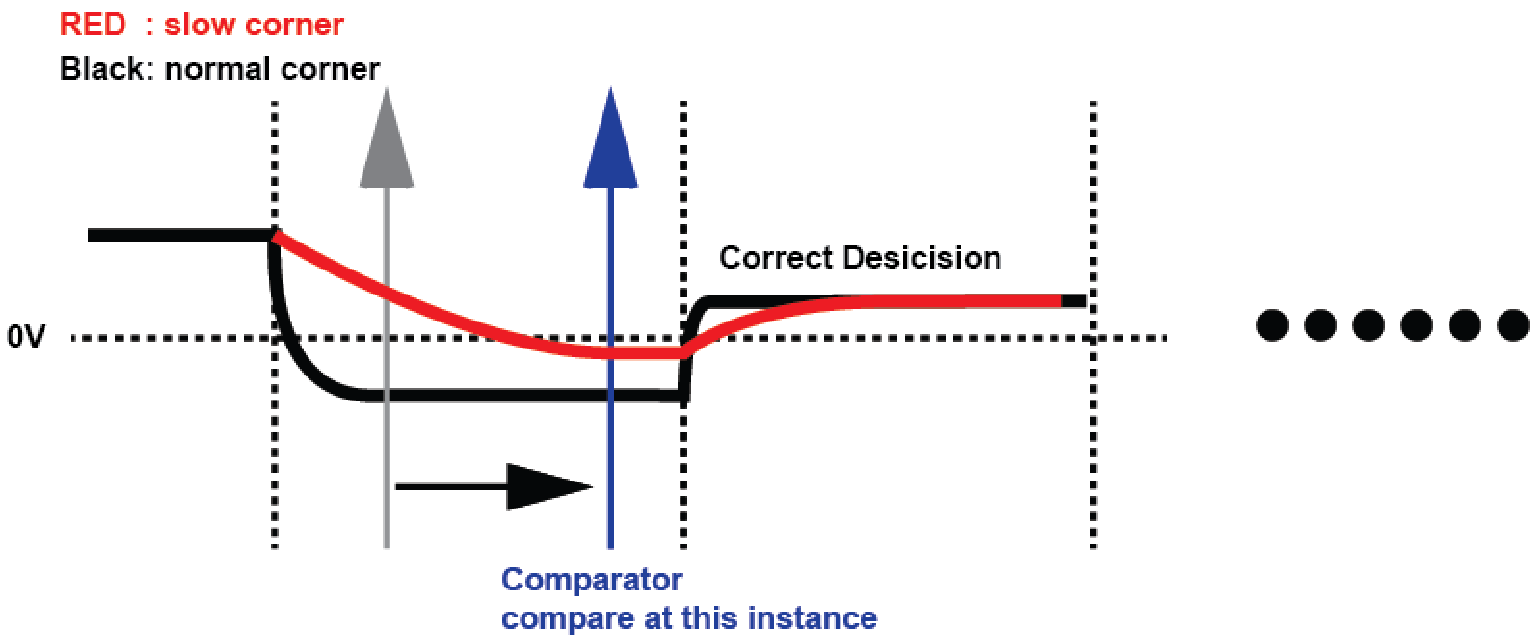
Tentative solution

Here shows the delay cell which I implemented.



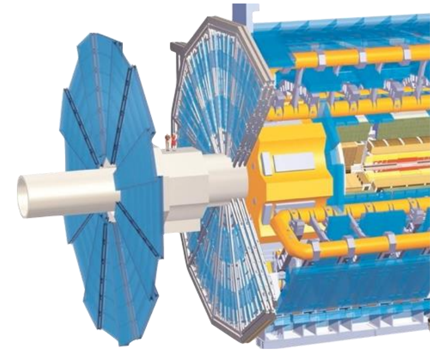
Tentative solution

Adding some supply controlled inverter to adjust comparator's activation instance



Future plan

- ADC is almost done now. Starting to do integration layout with Jaro, Sarthak, and Ray.



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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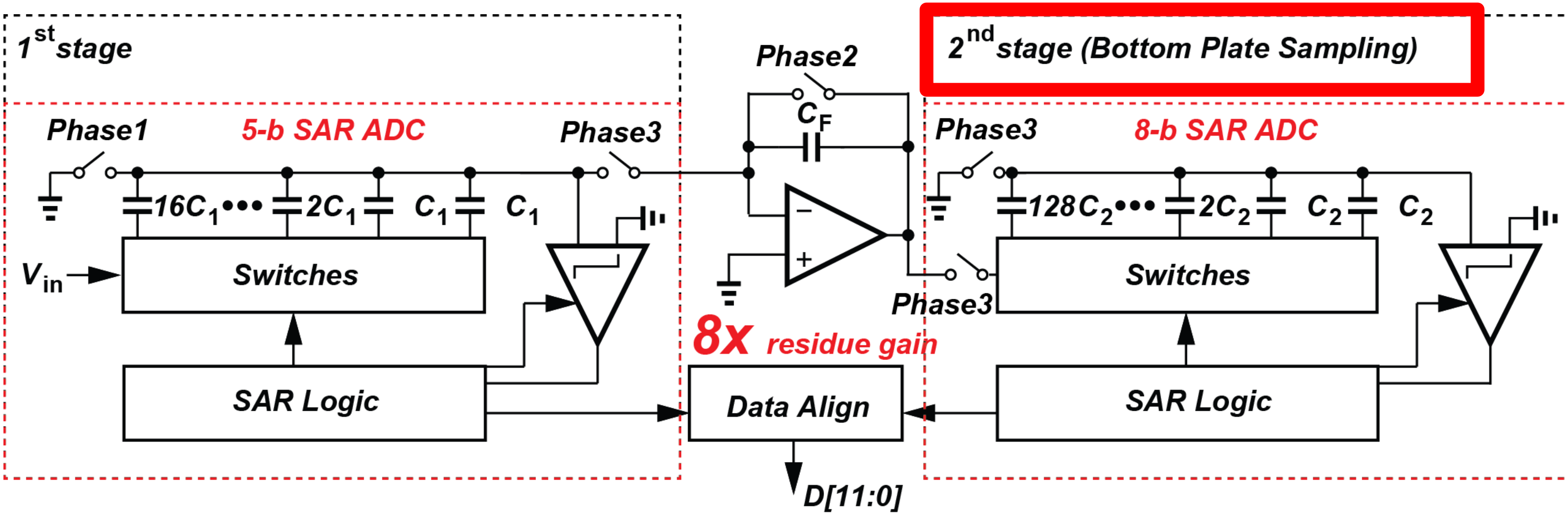
April 24, 2017

Review



- Second stage switches to bottom plate sampling instead of top plate sampling.

Simulation results

Simulation in new verison ADC

Pre-sim Corner(45 corner) with bond wire and noise	Done
Post-sim c+cc for 2nd stage and amp	Done
Post-sim c+cc for 1st stage	Done
Post-sim c+cc for with whole chip	Done
Post-sim corner (45 corner)	Some corner fails

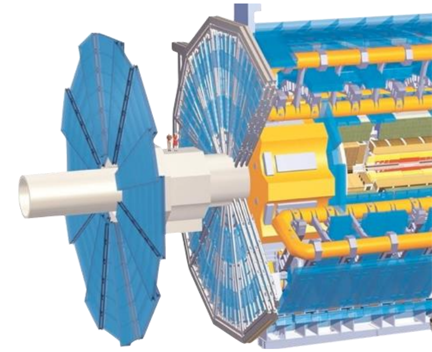
45 corners simulated with C+CC without noise

Parameter	C0_2	C0_2	C0_2	C0_2	C0_0	C0_1	C0_2
Model Group	TT	FF	FS	SF	SS	SS	SS
VDD	1.08	1.08	1.08	1.08	1.08	1.08	1.08
temperature	80	80	80	80	-20	27	80
Output	**C0_2**	**C0_2**	**C0_2**	**C0_2**	**C0_0**	**C0_1**	**C0_2**
/DOUT							
spectrum_enob	10.71	10.21	10.06	10.49	9.541	10.11	9.719
spectrum_sinad	66.25	63.2	62.31	64.94	59.2	62.63	60.27
spectrum_snr	66.25	63.2	62.31	64.94	59.2	62.63	60.27
spectrum_sfdr	73.69	69.48	69.49	71	66.23	68.6	67.14

- While operating at 5 corners shown above, ADC can not meet our spec.

Future plan

- Found out the problem and fix it.
- Then Run with 45 corners with noise on.



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

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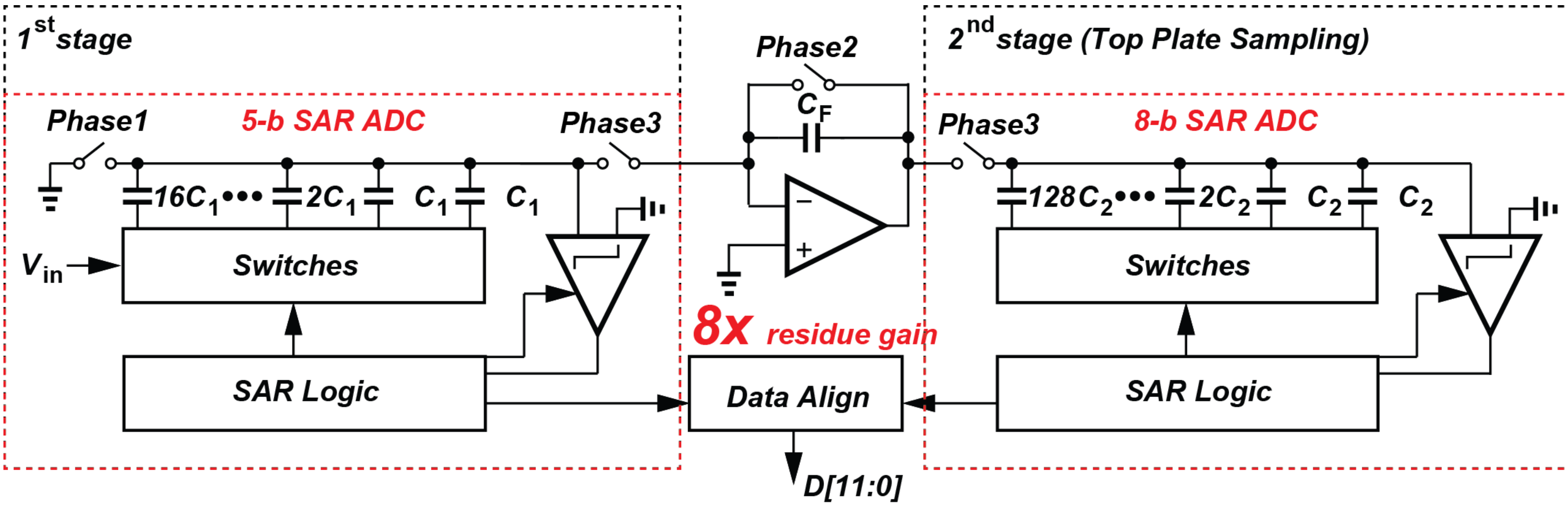
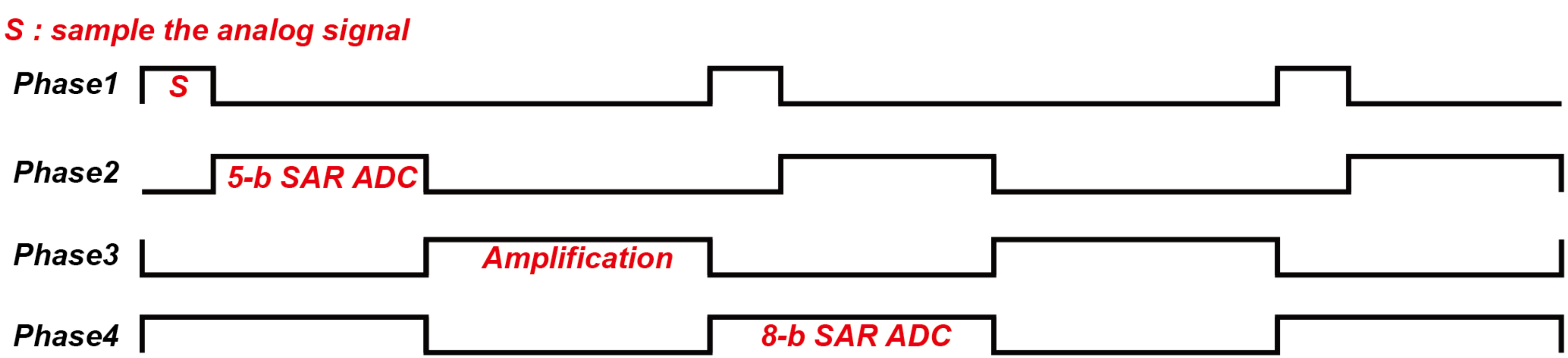
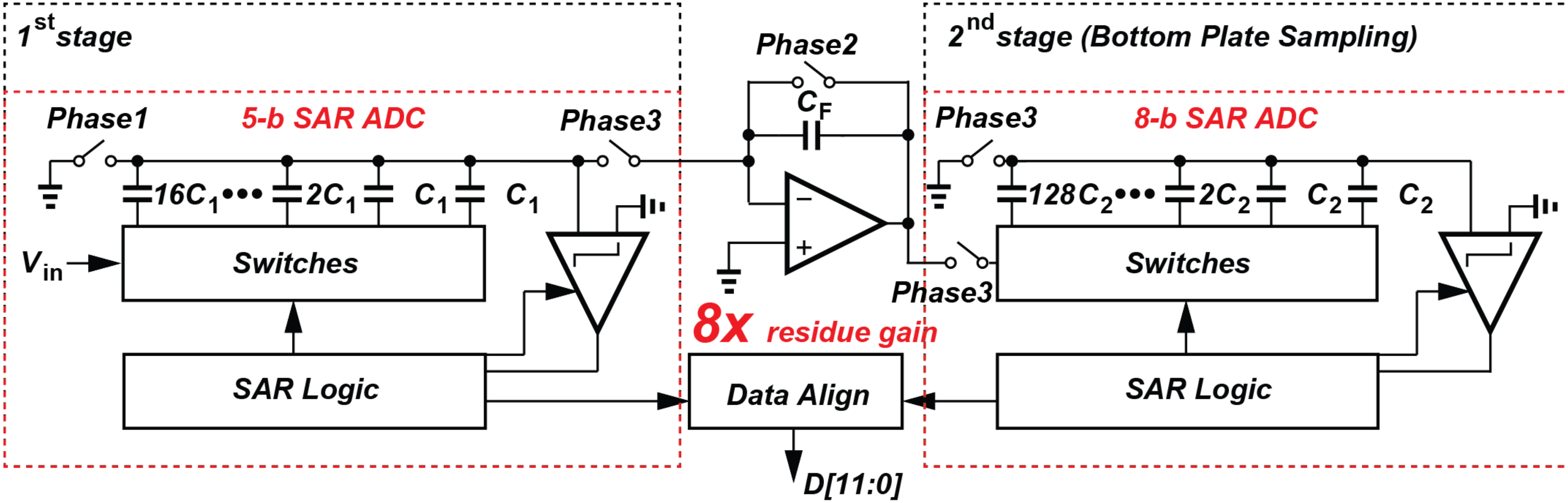
April 14, 2017

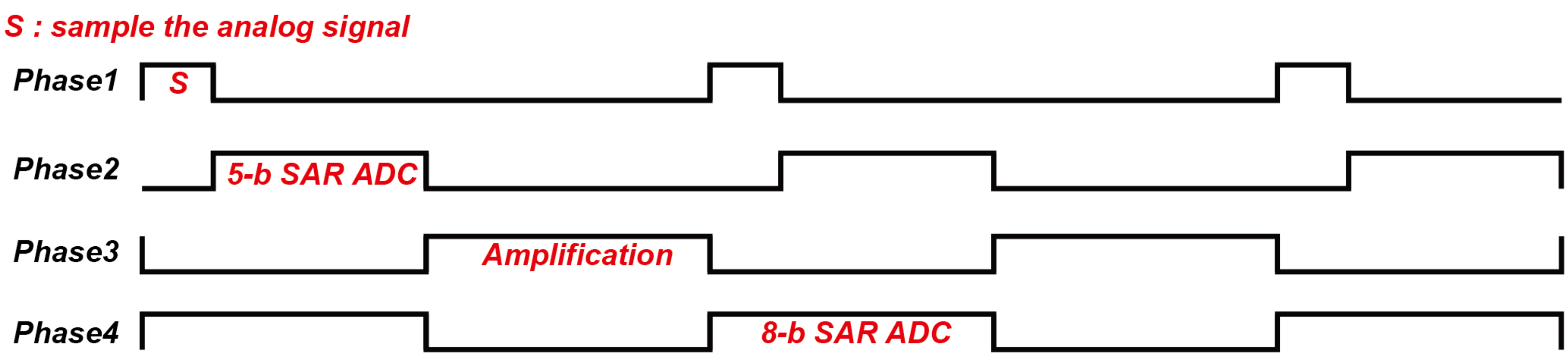
Architecture slightly change





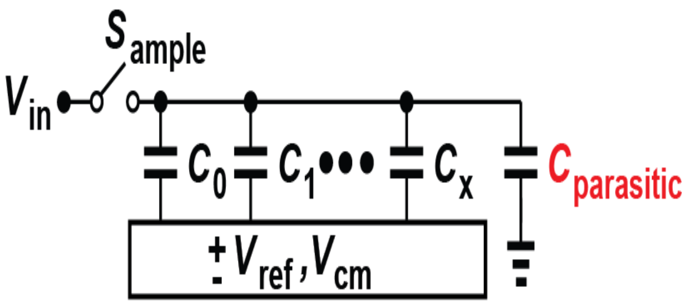
Architecture slightly change





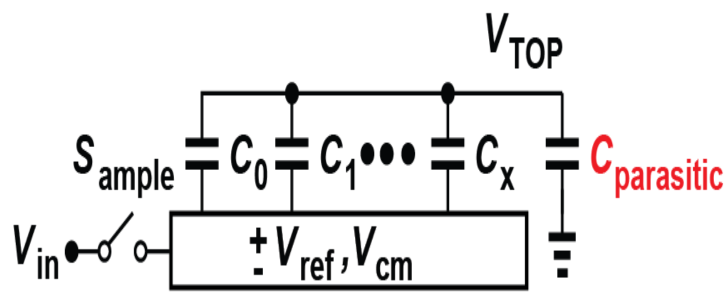
Effect of Top V.S. Bottom Sampling

Top Plate Sampling



$$V_{TOP} = V_{in} - \frac{b_1 C_1 \bullet\bullet\bullet + b_x C_x}{C_0 + C_1 \bullet\bullet\bullet + C_x + C_{parasitic}} V_{ref}$$

Bottom Plate Sampling



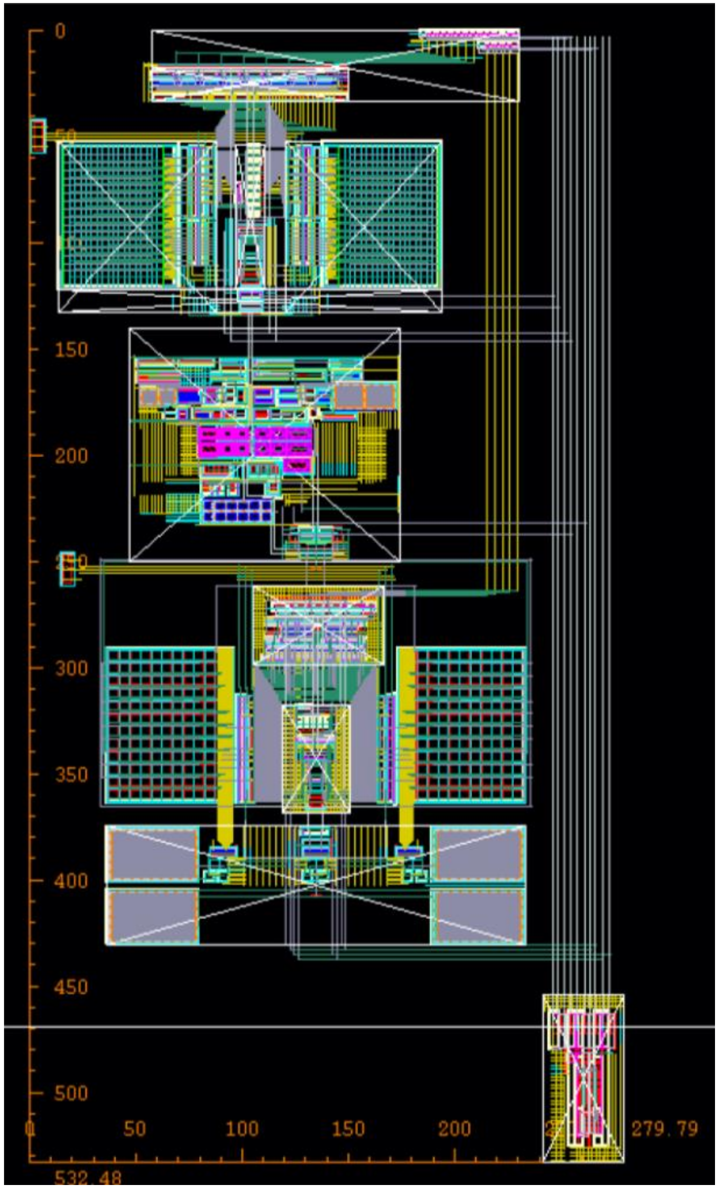
$$V_{TOP} = \underbrace{\left(V_{in} - \frac{b_1 C_1 \bullet\bullet\bullet + b_x C_x}{C_0 + C_1 \bullet\bullet\bullet + C_x} V_{ref} \right)}_{\textit{Ideal Term}} \frac{C_0 + C_1 \bullet\bullet\bullet + C_x}{C_0 + C_1 \bullet\bullet\bullet + C_x + C_{parasitic}}$$

Simulation planned to do

Simulation in new verison ADC

Pre-sim Corner(45 corner) with bond wire and noise	Simulate it again
Post-sim c+cc for 2nd stage and amp	Simulate it again
Post-sim c+cc for 1st stage	Simulate it again
Post-sim c+cc for with whole chip	Simulate it again
Post-sim corner (45 corner)	Simulate it again

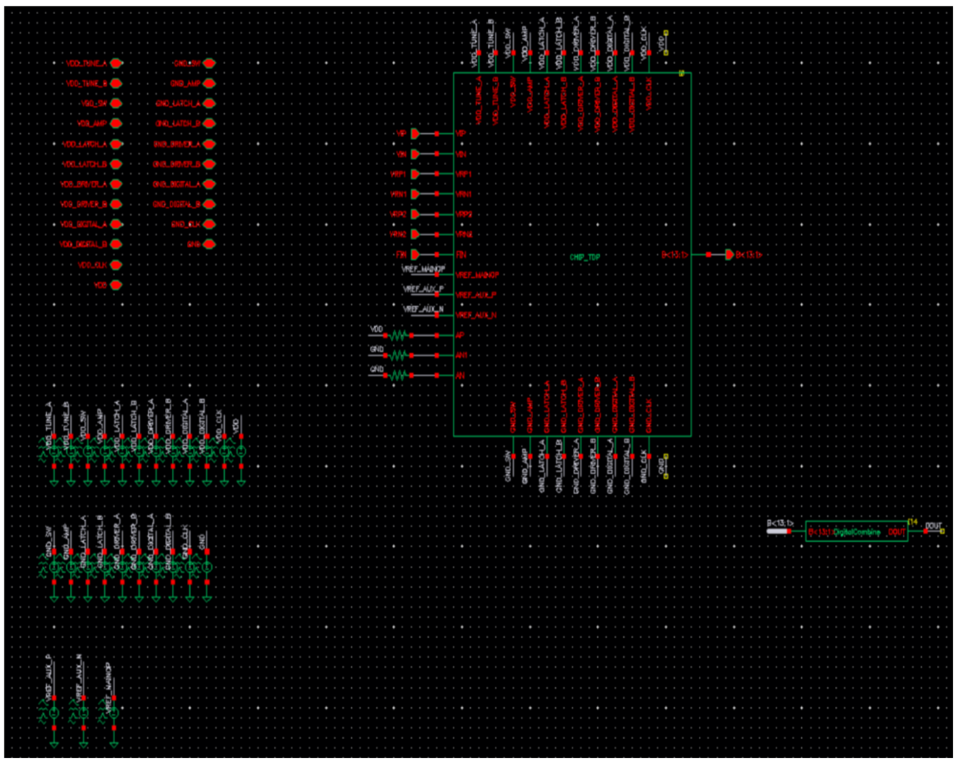
Layout for core circuit



Area	
Core	279.79um * 532.48um

TOP Level

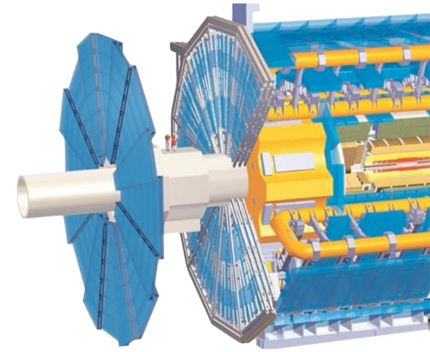
Top Module is located at
/home/ckhsu/TSMC65LP/CHIP_TOP



Signal PAD	2
Reference PAD	4
CLK PAD	1
OP_CMFB	3
OP_BIAS	3
VDD&GND	9&9
Delay Tuning	2
Digital Output	13
Total	46

Future Plan

- Complete the Simulation.
- Discuss integrated simulation with Sarthak, Jaros , and Ray.



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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April 7, 2017

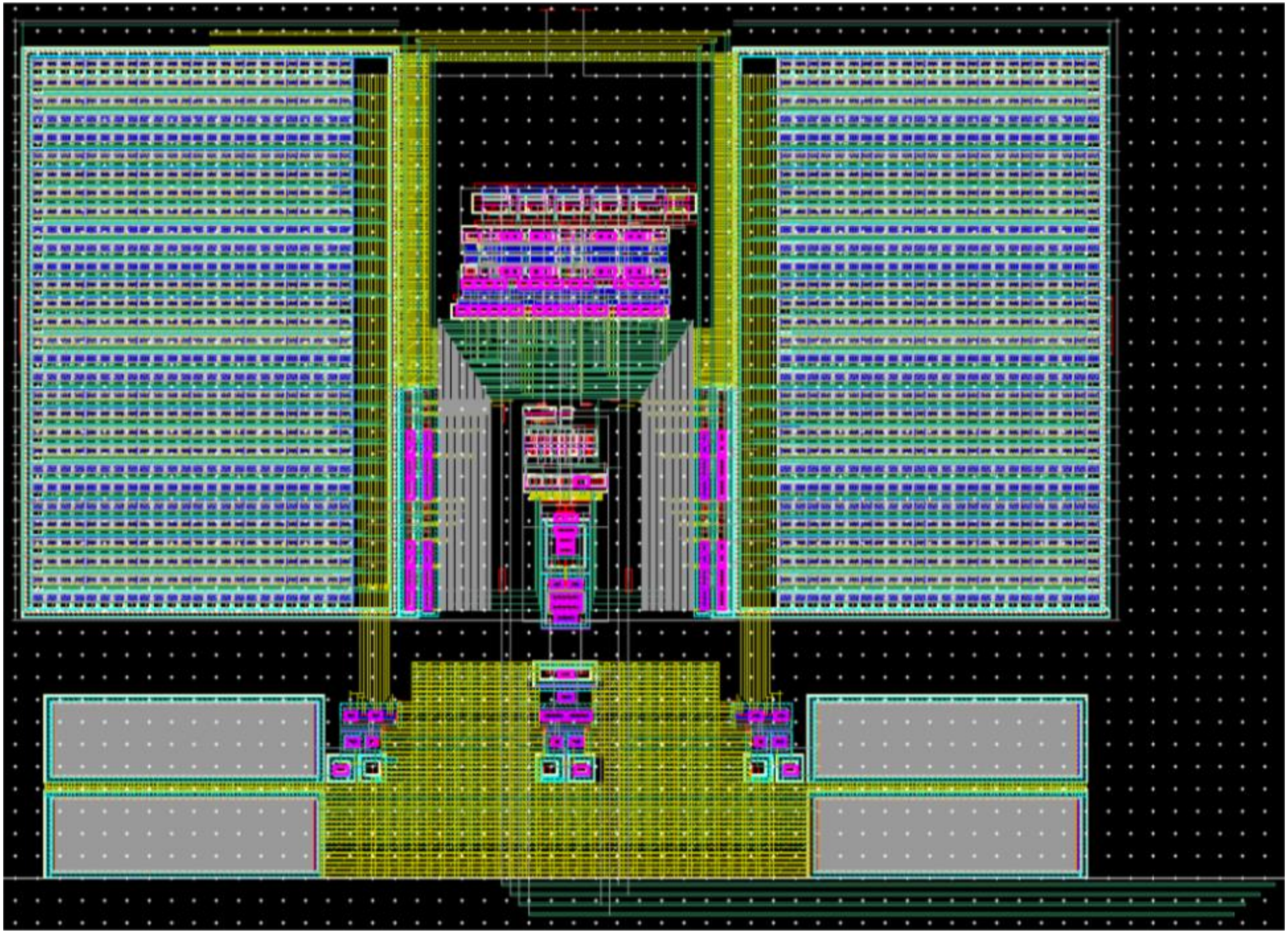
Layout Status Update

12-b Pipeline SAR	Status(Up to date)	Status(before last week)
Whole Chip	Almost Done	Haven't Done
1st stage SAR ADC	Done	Haven't Done
Amplifier	Done	Done
2nd stage SAR ADC	Done	Done
CLK Buffer	Done	Done

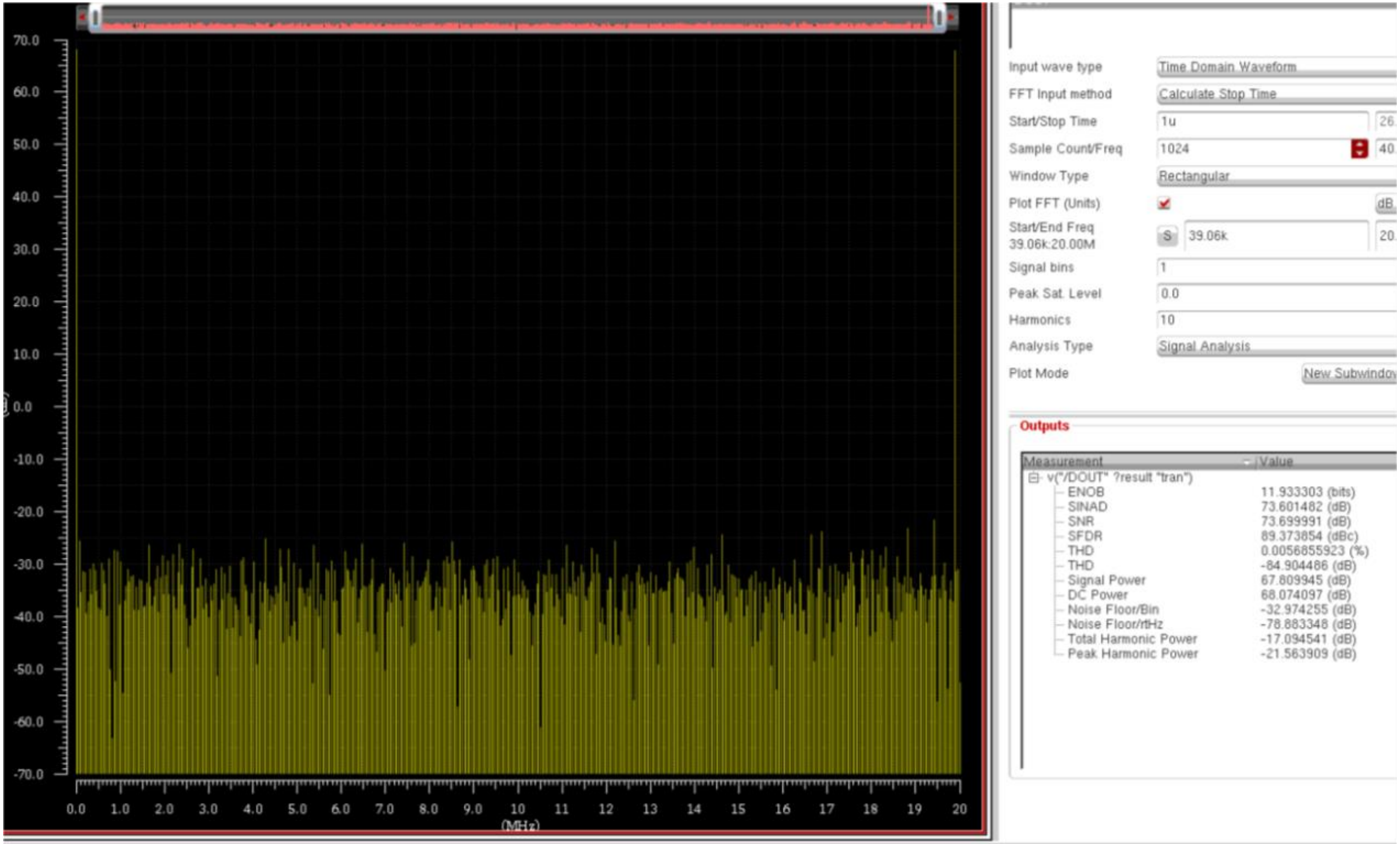
Simulation I did

	Simulation
Pre-sim Corner(45 corner) with bond wire and noise	Pass
Post-sim c+cc for 2nd stage and amp	Pass
Post-sim c+cc for 1st stage	Pass
Post-sim c+cc for with whole chip	Haven't done it
Post-sim corner (45 corner)	Haven't done it

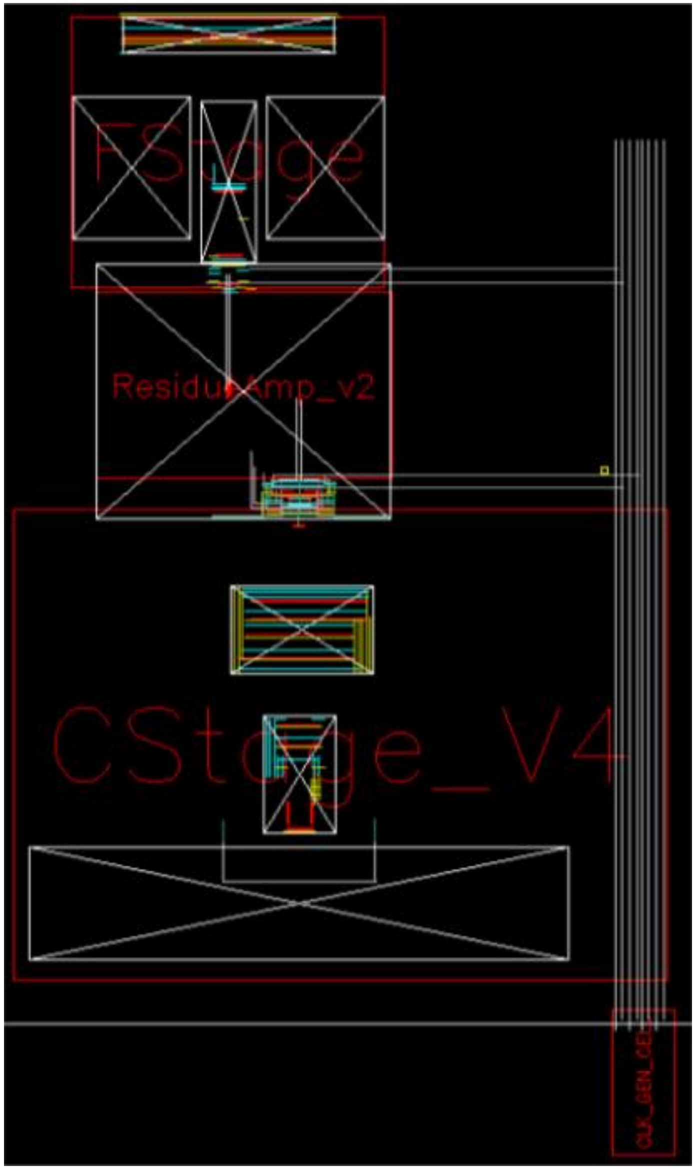
Firs stage Layout

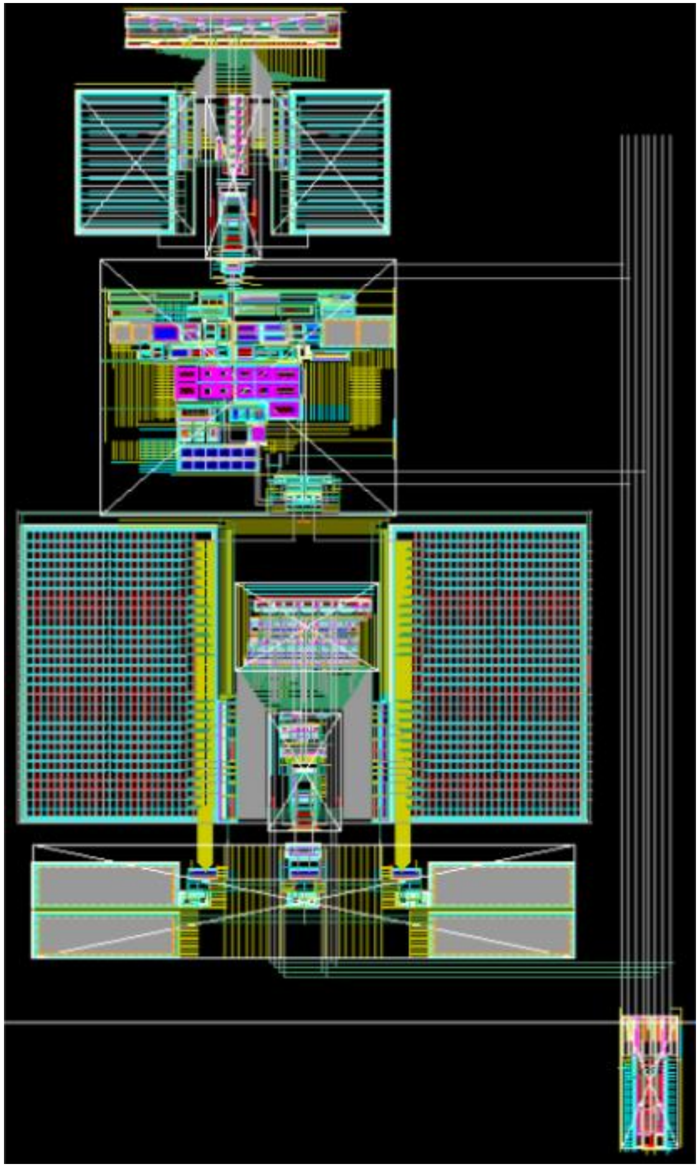


Firs stage c+cc simulation (wo noise)



Layout for whole circuit





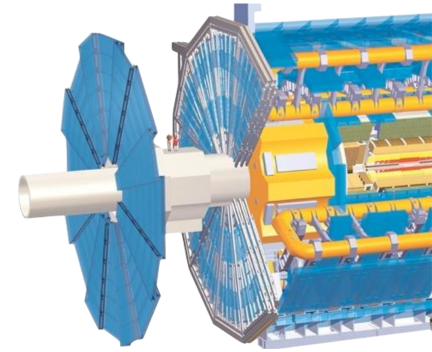
Future plan & Problem

◆Future plan:

- Provide the top symbol to nevis server for integration simulation by this weekend.
- Run C+C simulation for entire chip.
- Run R+C+CC simulation if time allows.

◆Problem:

- Very slow connection from UT side to access the nevis server while opening the virtuoso.



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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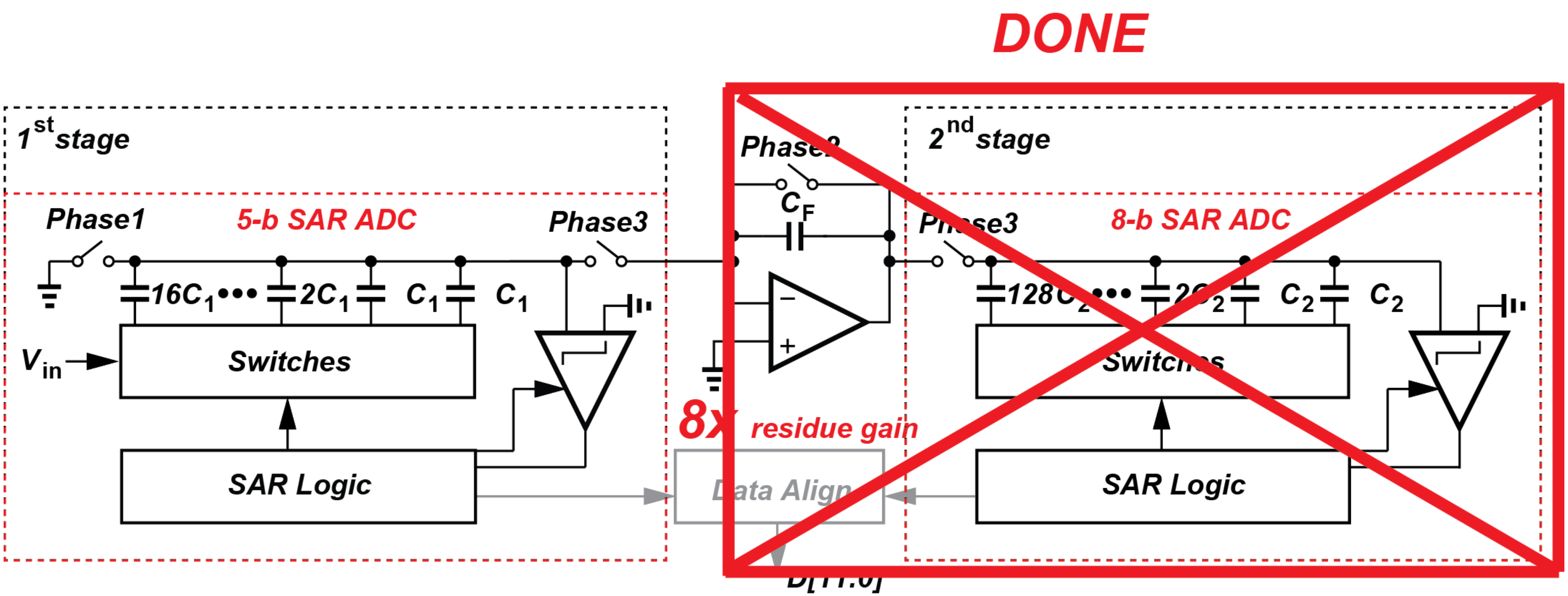
March 24, 2017

Layout status



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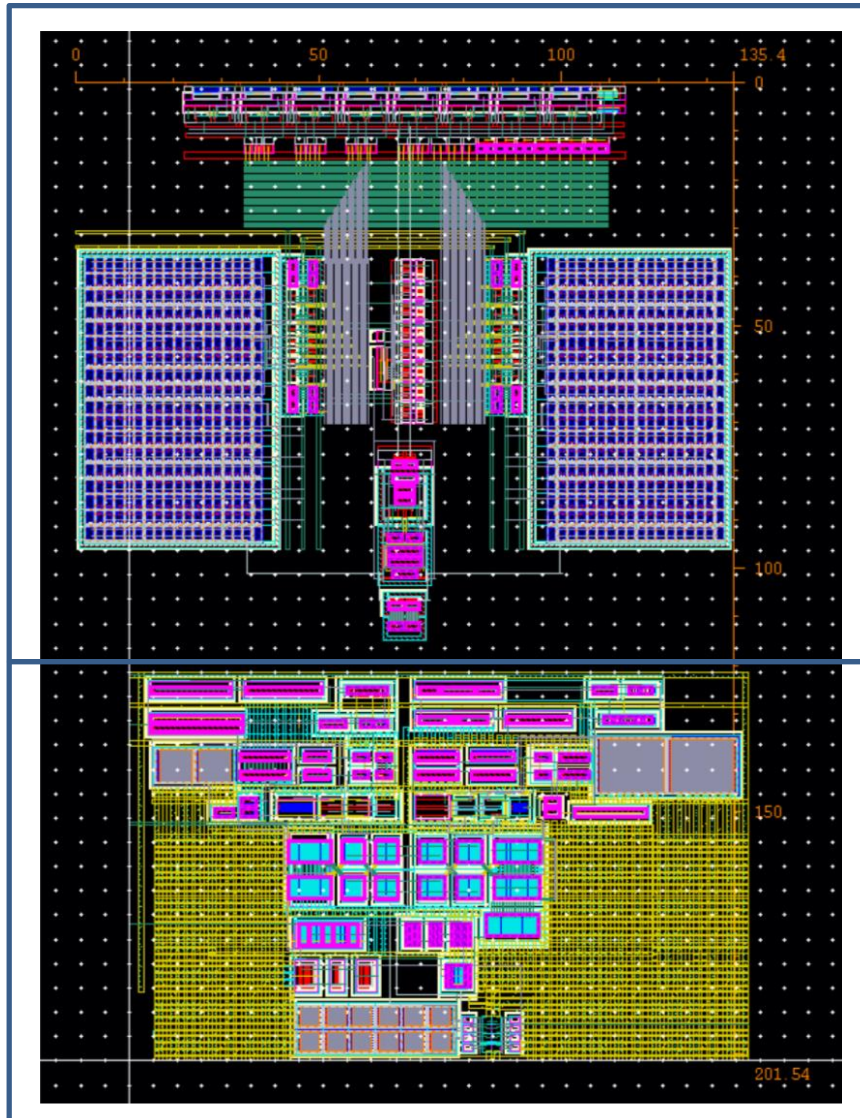
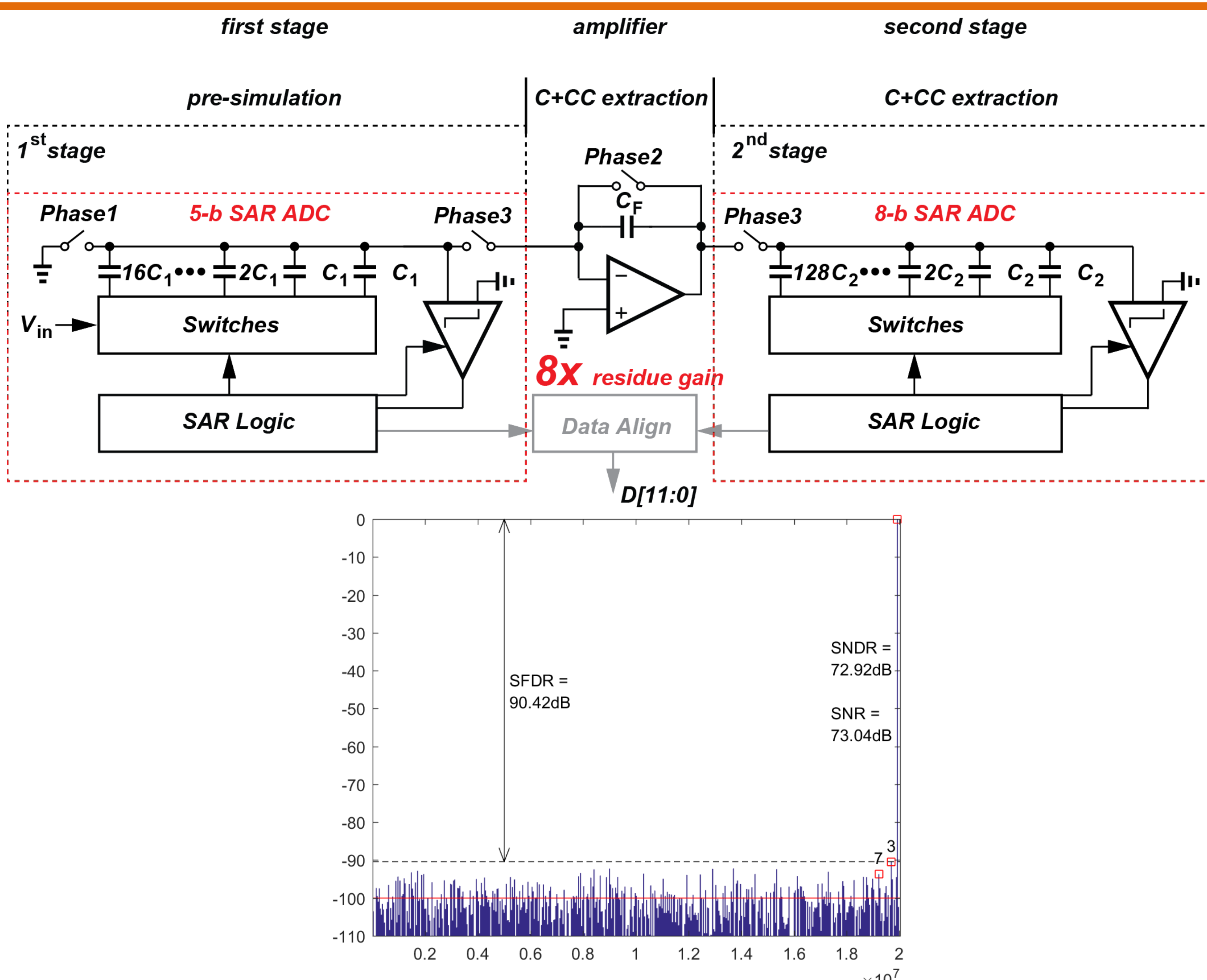
Layout Update

ATLAS
EXPERIMENT

2nd stage ADC

Amplifier



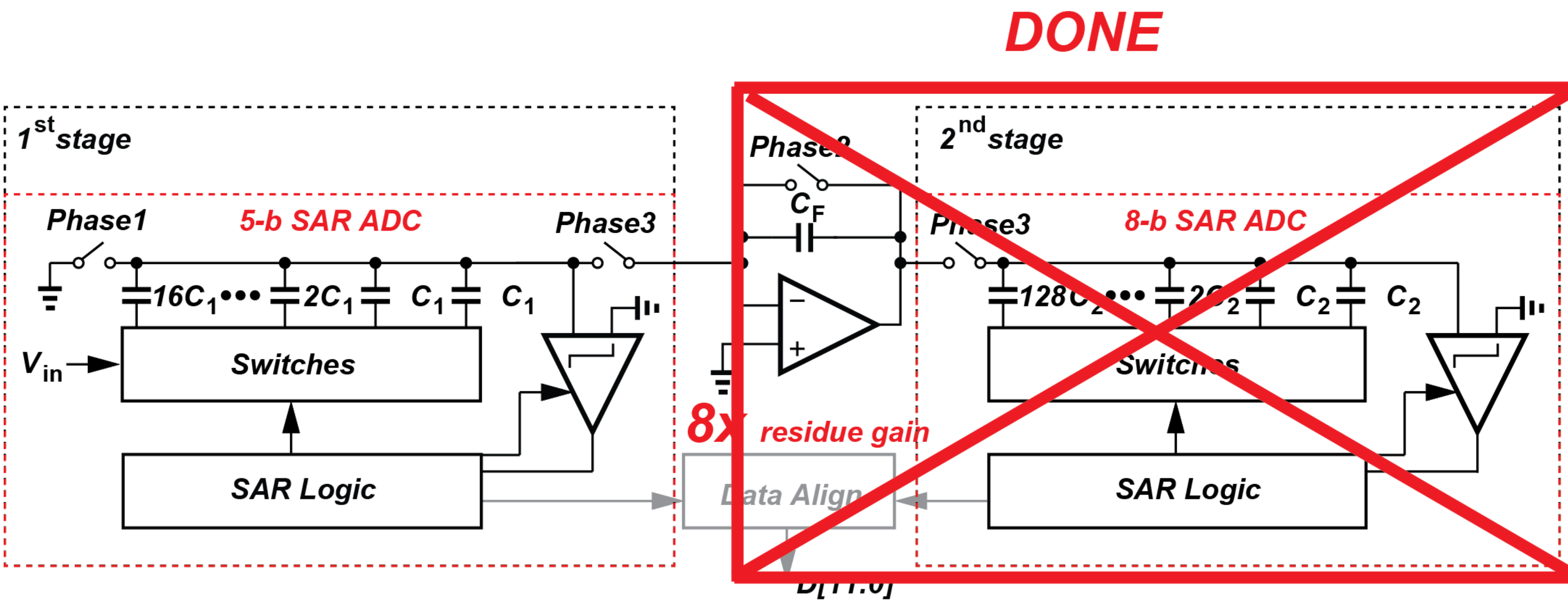

first stage
amplifier
second stage
pre-simulation
C+CC extraction
C+CC extraction
1st stage
2nd stage
Phase2
Phase1
5-b SAR ADC
Phase3
Phase3
8-b SAR ADC
C_F
$16C_1$ ••• $2C_1$ C_1 C_1
$128C_2$ ••• $2C_2$ C_2 C_2
V_{in}
Switches
Switches
SAR Logic
SAR Logic
8x residue gain
Data Align
D[11:0]
SFDR = 90.42dB
SNDR = 72.92dB
SNR = 73.04dB
$\times 10^7$

Corner Simulation

	ENOB @ 80 degree and 1.2V	ENOB @ -20 degree and 1.2V
TT	11.84	11.86
SS	11.83	11.74
FF	11.63	11.85
FS	11.74	11.82
SF	11.8	11.88

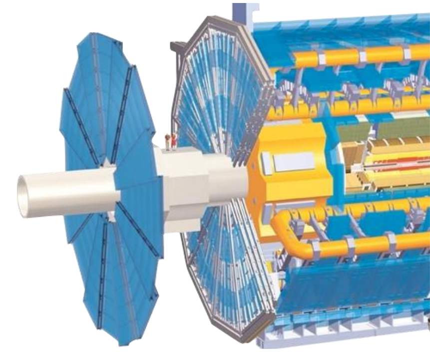
	ENOB @ 80 degree and 1.32V	ENOB @ -20 degree and 1.32V
TT	11.75	11.76
SS	11.86	11.86
FF	11.61	11.84
FS	11.53	11.65
SF	11.81	11.81

Future Plan



- Finish the first stage by the end of this week
- Finish the whole circuit routing by the end of this month.

The University of Texas at Austin



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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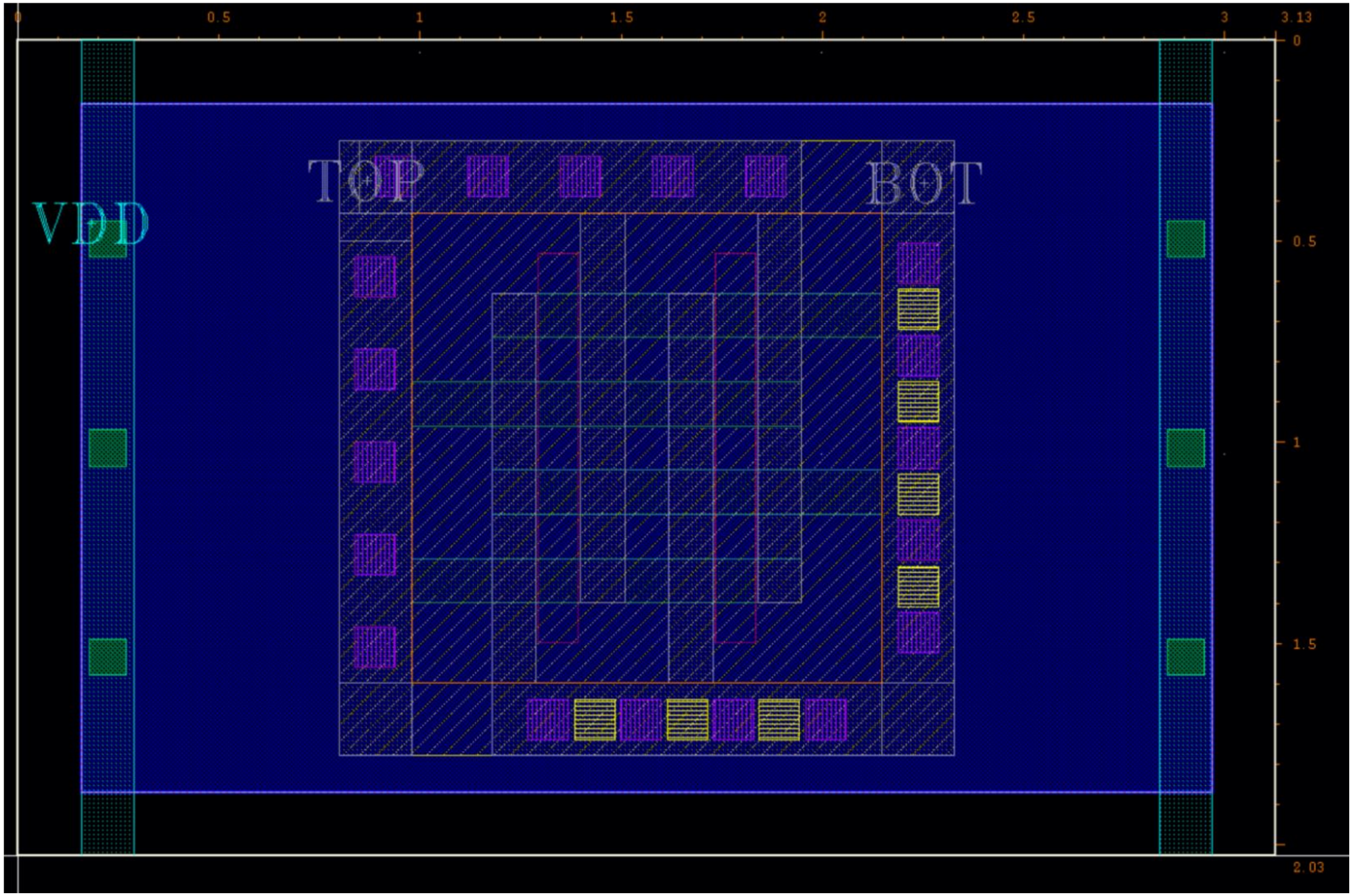
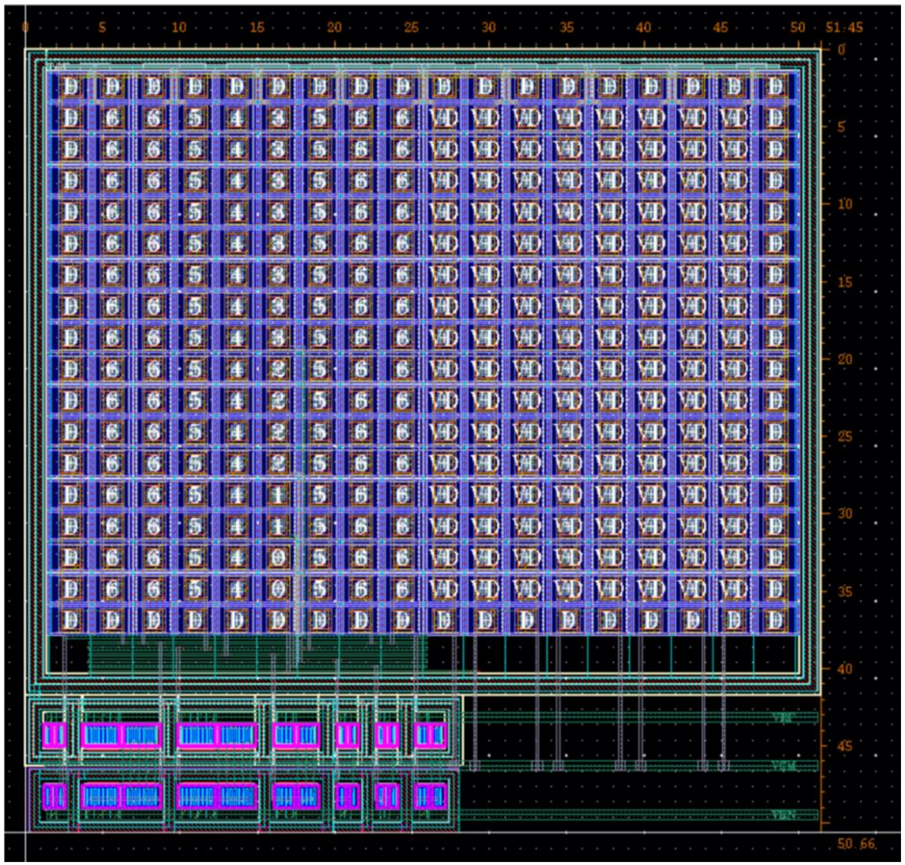
March 17, 2017

Customized Cap for second stage



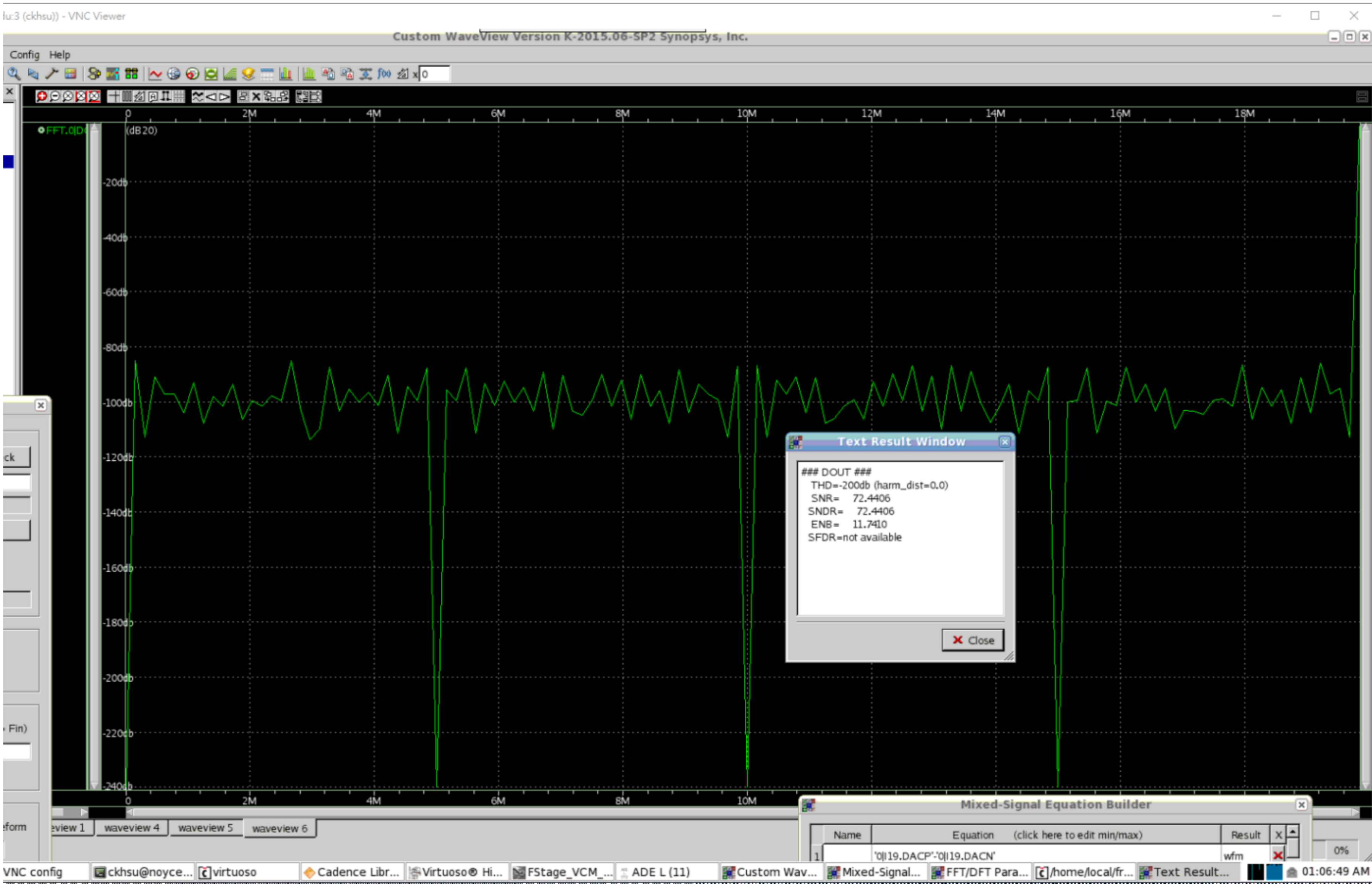
- Shielding the top plate in order to reduce the parasitic.

Fstage Dac Array

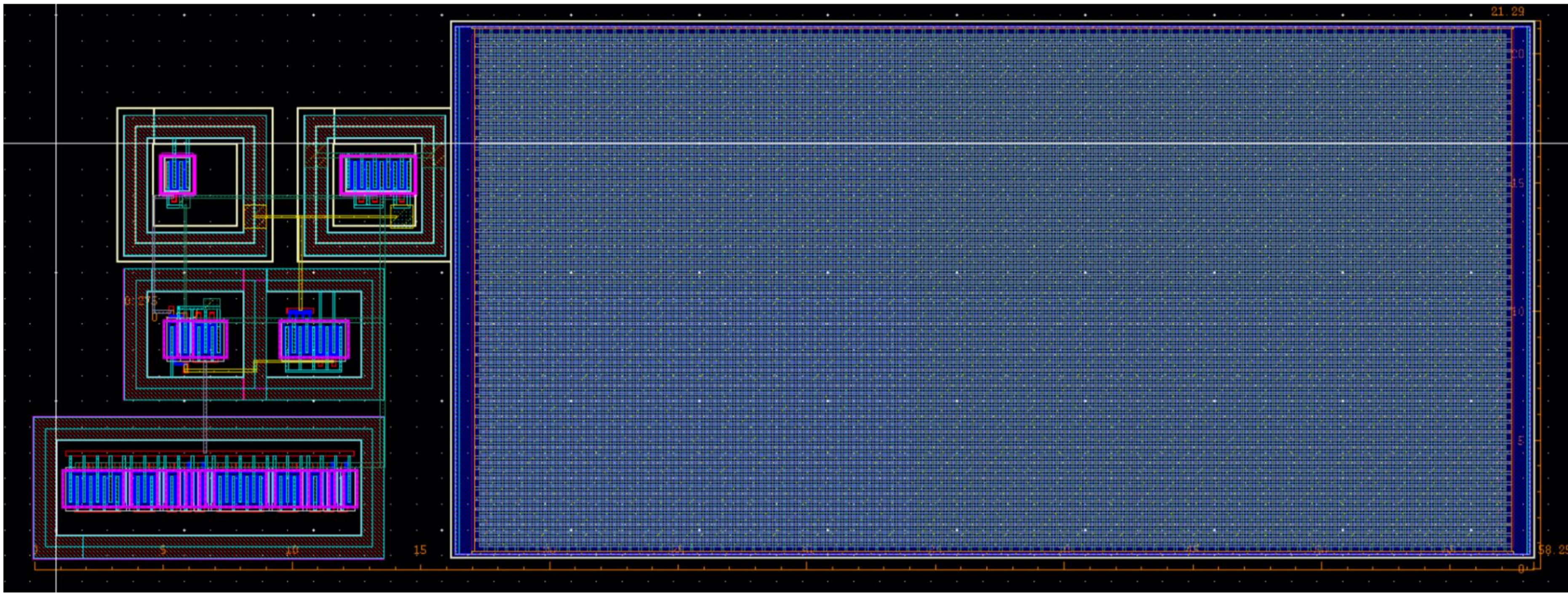


	Capacitance(fF)	Normalized(fF)
B7	66.1476	63.8
B6	33.1085	31.97
B5	16.5783	16.00
B4	8.28950	8.00
B3	4.14297	4.00
B2	2.06862	1.997
B1	1.03556	1

256 points

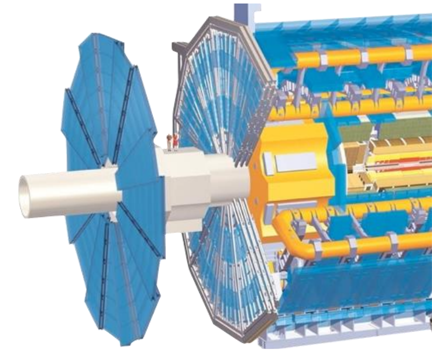

Custom WaveView Version K-2015.06-SP2 Synopsys, Inc.
Config Help
(dB20)
-20db
-40db
-60db
-80db
-100db
-120db
-140db
-160db
-180db
-200db
-220db
-240db
0 2M 4M 6M 8M 10M 12M 14M 16M 18M
Text Result Window
DOUT
THD=-200db (harm_dist=0.0)
SNR= 72.4406
SNDR= 72.4406
ENB= 11.7410
SFDR=not available
Close
Mixed-Signal Equation Builder
Name
Equation (click here to edit min/max)
Result
'0|I19.DACP'-'0|I19.DACN'
wfm
waveview 4
waveview 5
waveview 6
01:06:49 AM

Bootstrap SW



Future Plan

- Optimize the capacitor array ratio for 2^{nd} stage.
- Finish the 2^{nd} stage layout by the end of this week.
- Finish the 1^{st} stage layout by the end of next week.
- Whole chip routing by the end of this month.



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

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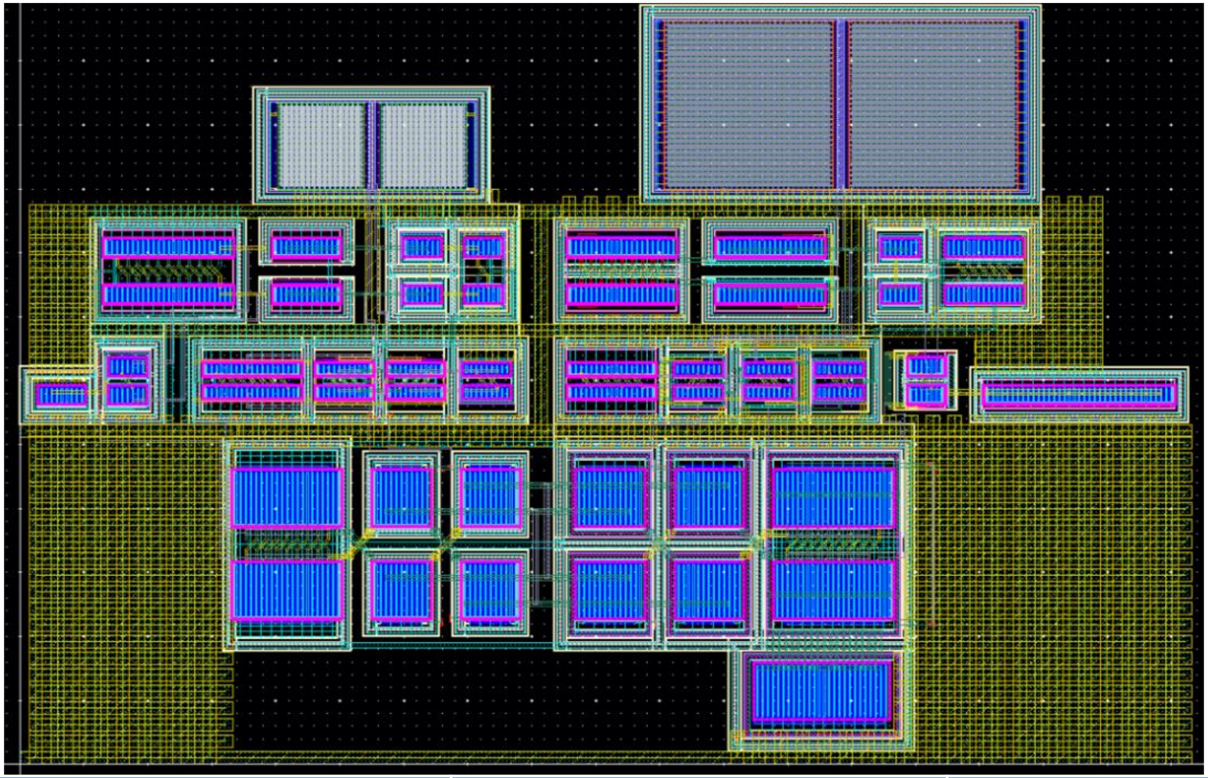
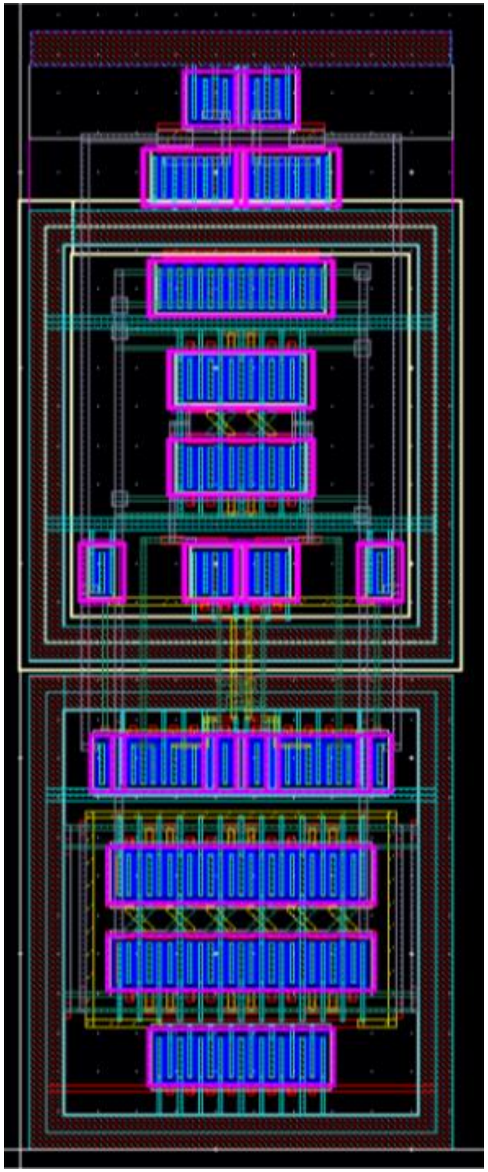
March 3, 2017

Layout(OPAMP)



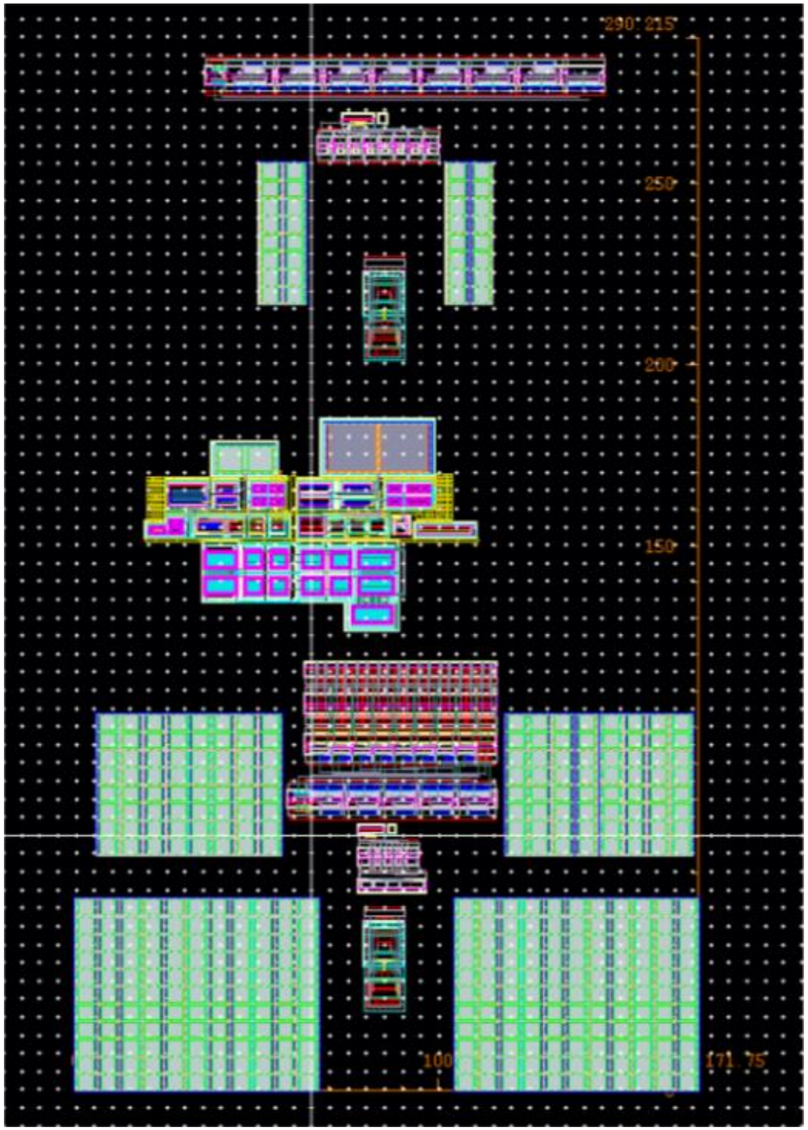
	Pre-Sim	Pos-sim(R+C+CC)
Supply Voltage	1.2 V	1.2 V
DC Gain	90.25dB	89.71 dB
PhaseMargin	67 degree	65 degree
Unit-Gain Freq	2.642GHz	2.25GHz

Layout(Comparator)



	Pre-sim	Pos-sim(R+C+CC)
Offset	0	960 uV
Noise	300 uV	260 uV

Floor Plan

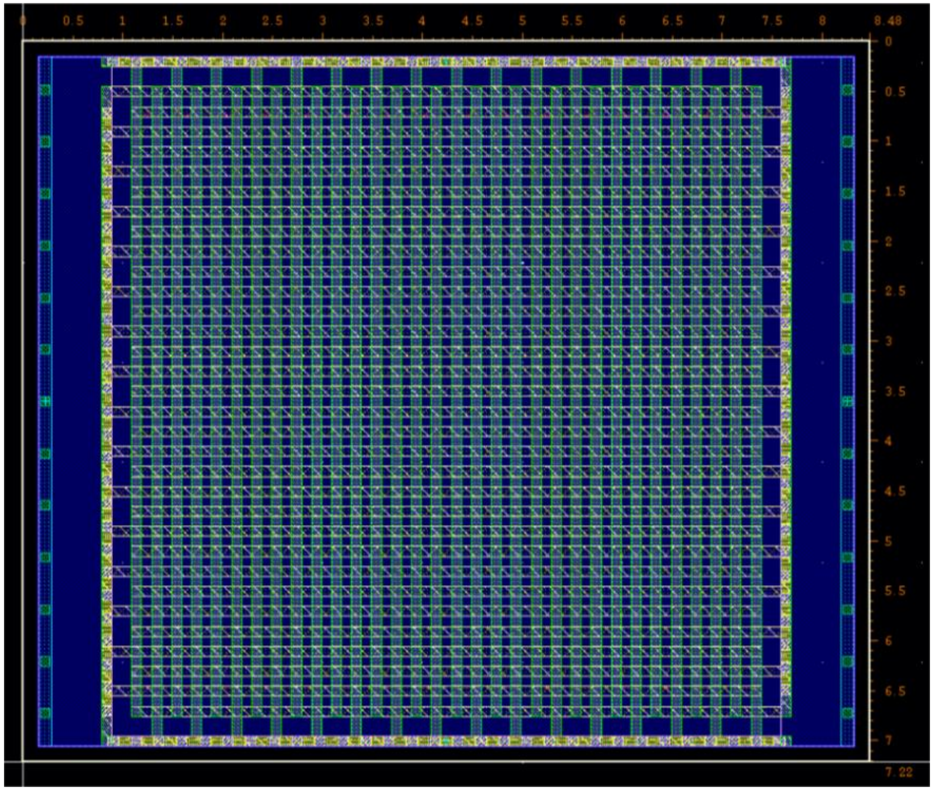


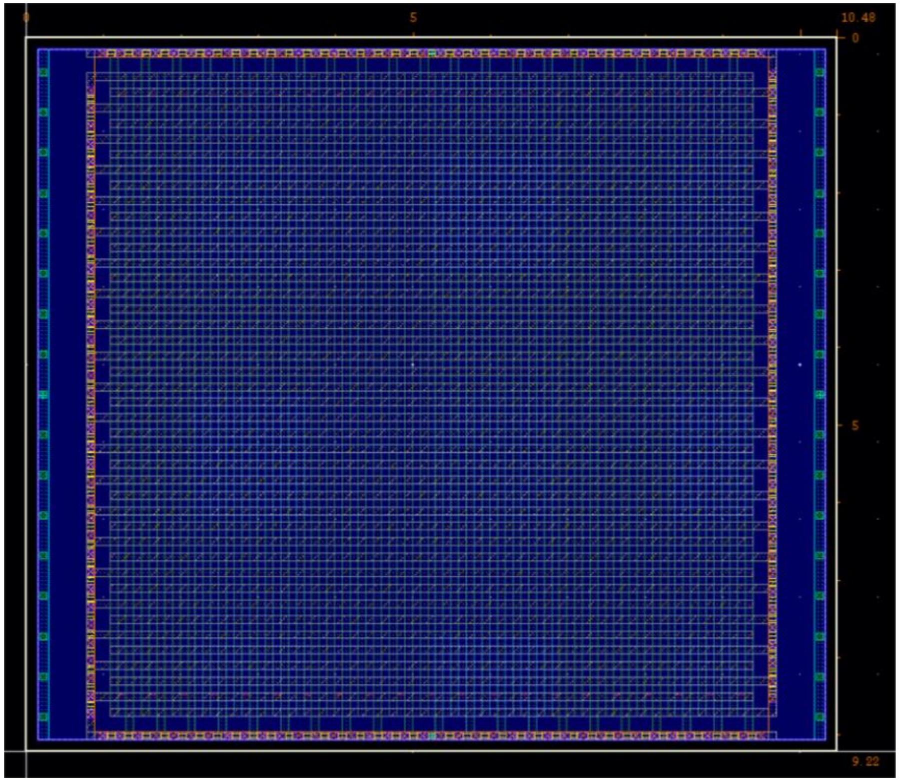
	Area
Stage 1	171um*120um
Stage 2	171um*100um
OPAMP	91um*60um
Core Area	171um*300um

Schedule

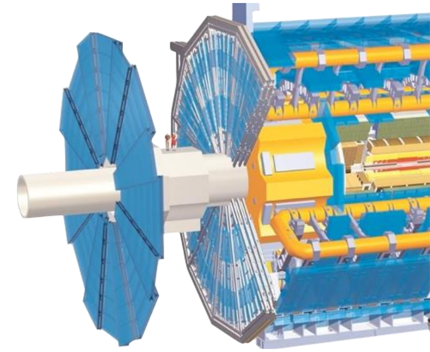
Now~2/28	March
✓ 1st Sar Logic ✓ 2nd Sar Logic ✓ CLK_GEN ✓ Comparator ✓ Amplifier Bootstrap SW DAC	Whole Chip routing & post-sim

1P9M or 1P6M





Same capacitance	1P9M	1P6M
Area(145fF)	8.5 um*7.3 um	10.5 um * 9.3 um



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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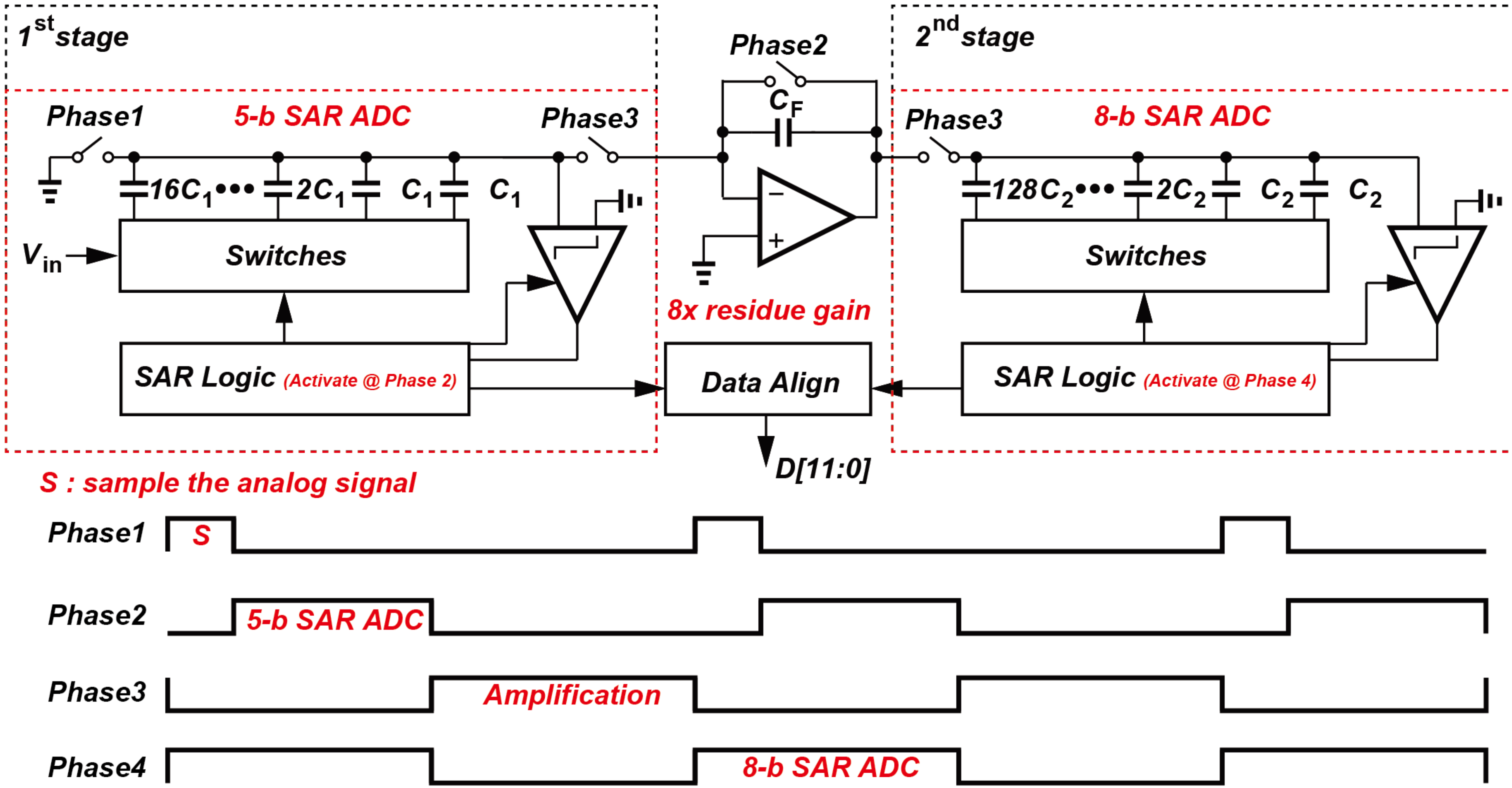
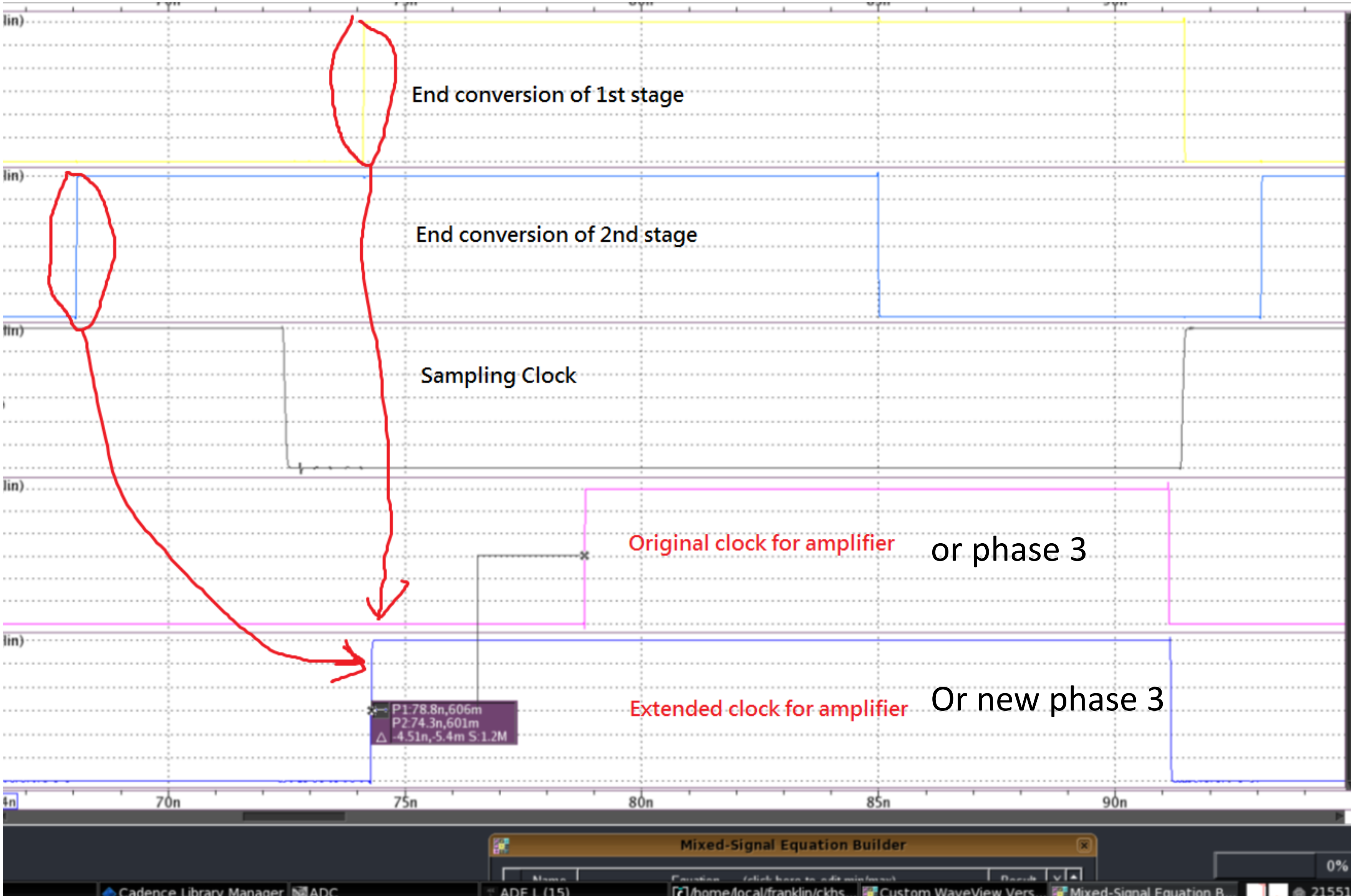
Feb 17, 2017

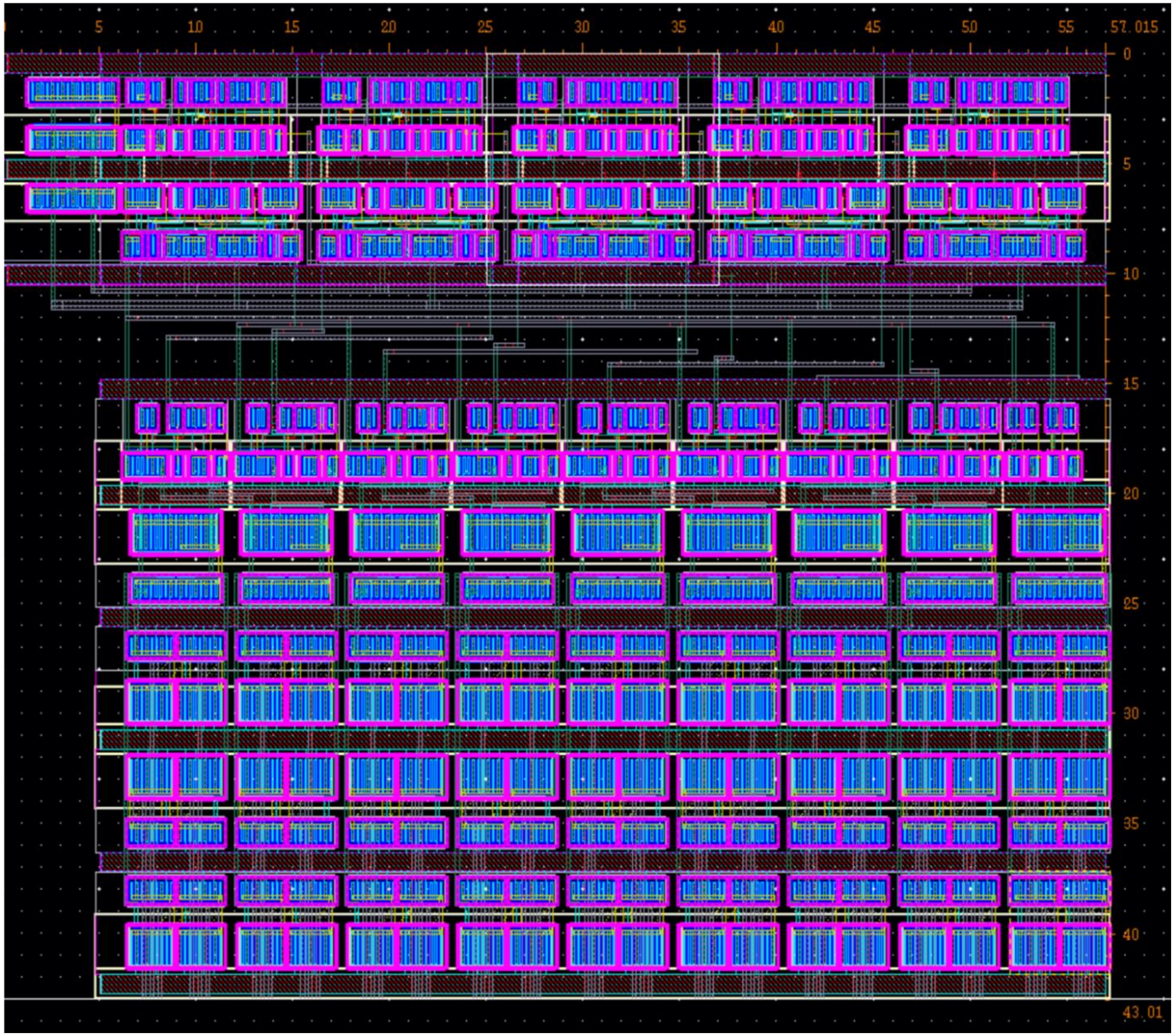
Adjustment on CLK Gen




End conversion of 1st stage
End conversion of 2nd stage
Sampling Clock
Original clock for amplifier
or phase 3
Extended clock for amplifier
Or new phase 3
P1:78.8n,606m
P2:74.3n,601m
△ -4.51n,-5.4m S:1.2M
70n
75n
80n
85n
90n
Mixed-Signal Equation Builder
Cadence Library Manager
ADC
ADE L (15)
/home/local/franklin/ckhs...
Custom WaveView Vers...
Mixed-Signal Equation B...

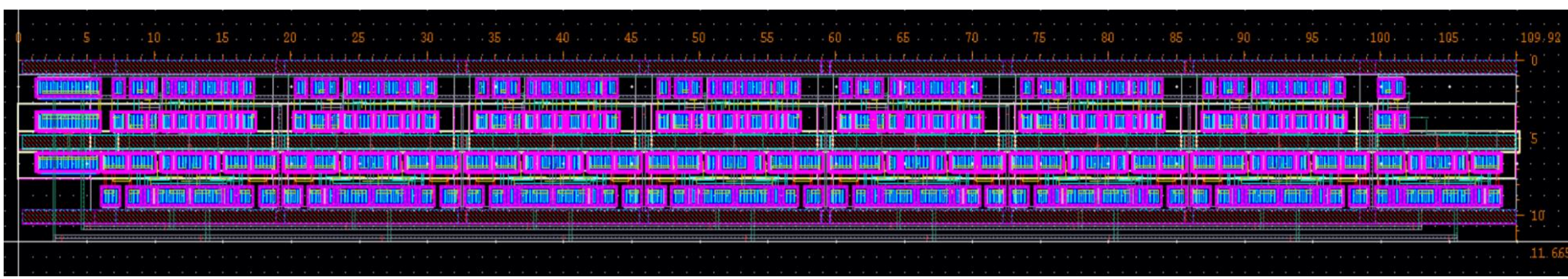
1st stage SAR logic

Area	51um*47um



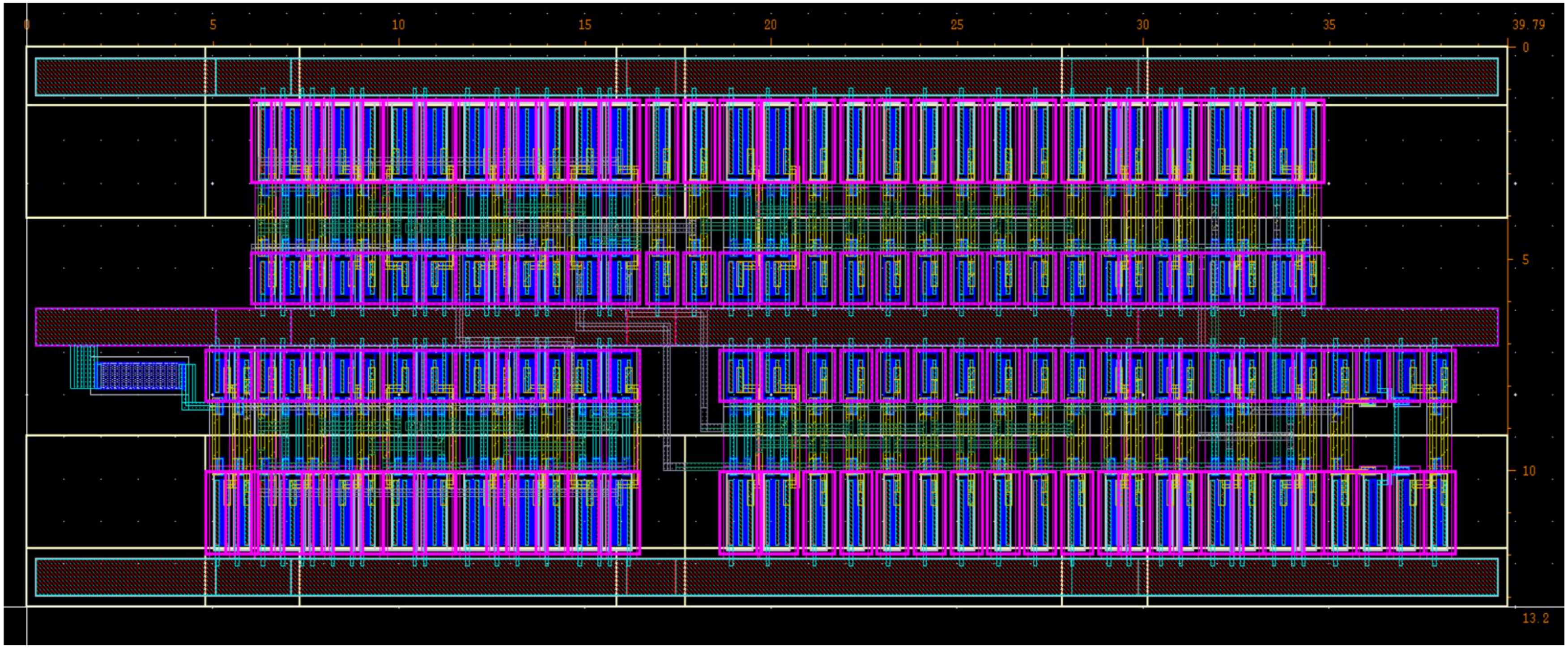
2nd stage SAR Logic

Area	109um*11um

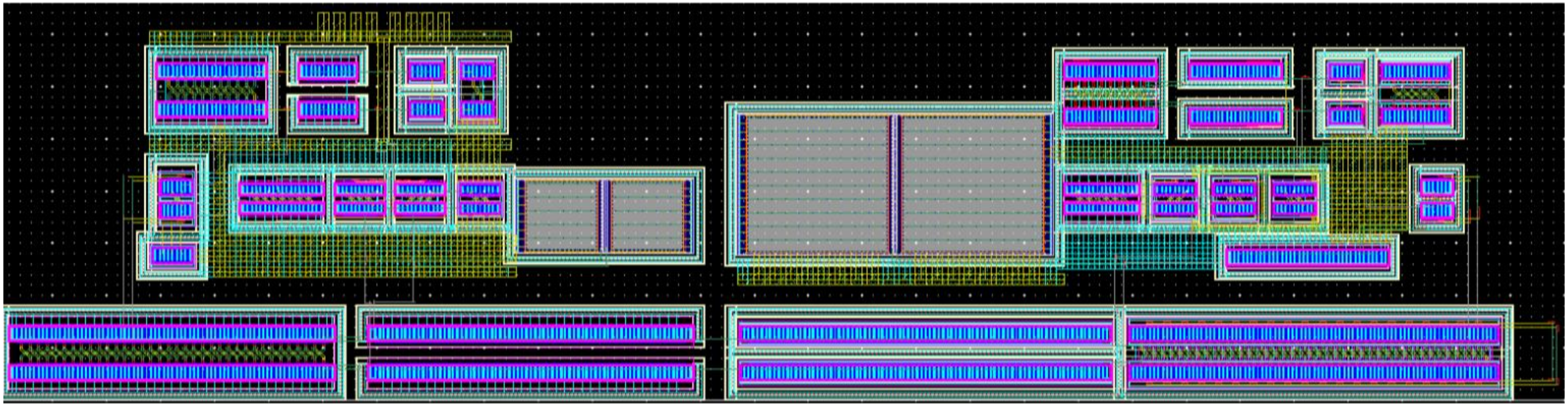


CLK_GEN

Area	39um*13um

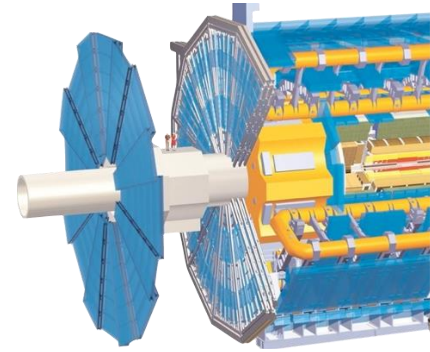


Amplifier(not finished)



Schedule

Now~2/28	March
1st Sar Logic 2nd Sar Logic CLK_GEN Comparator Amplifier Bootstrap SW DAC	Whole Chip routing & post-sim



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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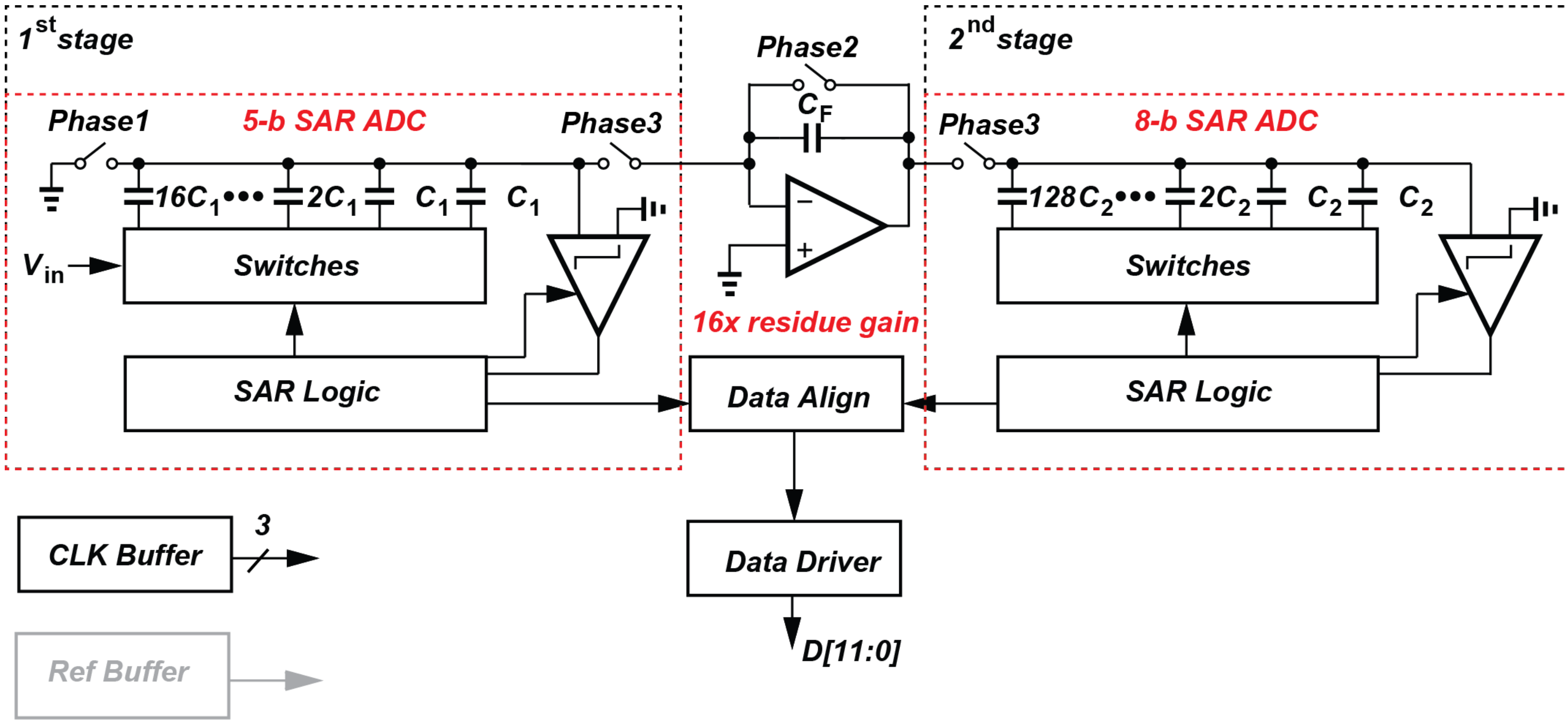
Jan 27, 2017

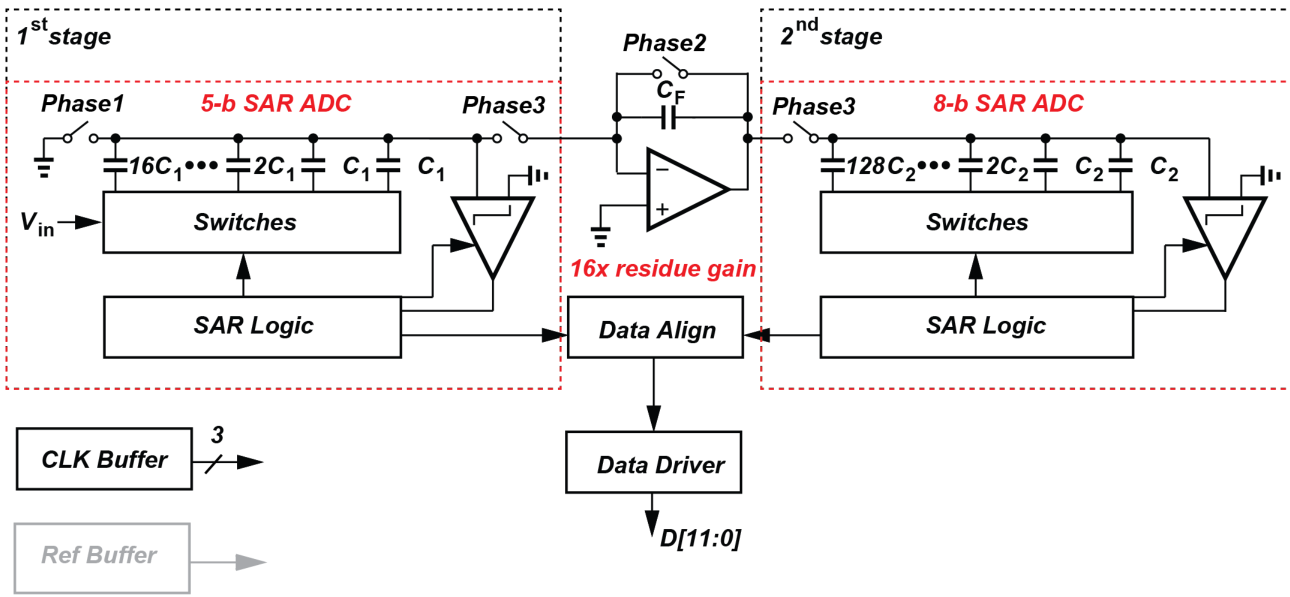
High Level review



ADC AND OPAMP Review

This ADC	Specification	OPAMP	Specification
Supply Voltage	1.2 V	Supply Voltage	1.2 V
Technology	TSMC 65LP	Technology	TSMC 65LP
Sampling Rate	40MS/s	DC Gain	87 dB
ENOB	11.66 bit	GBW	2.1 GHz
Power	4mW (no Ref Buffer)	Phase Margin	80 degree
Input capacitance	2pF single ended	Power	1.8 mW

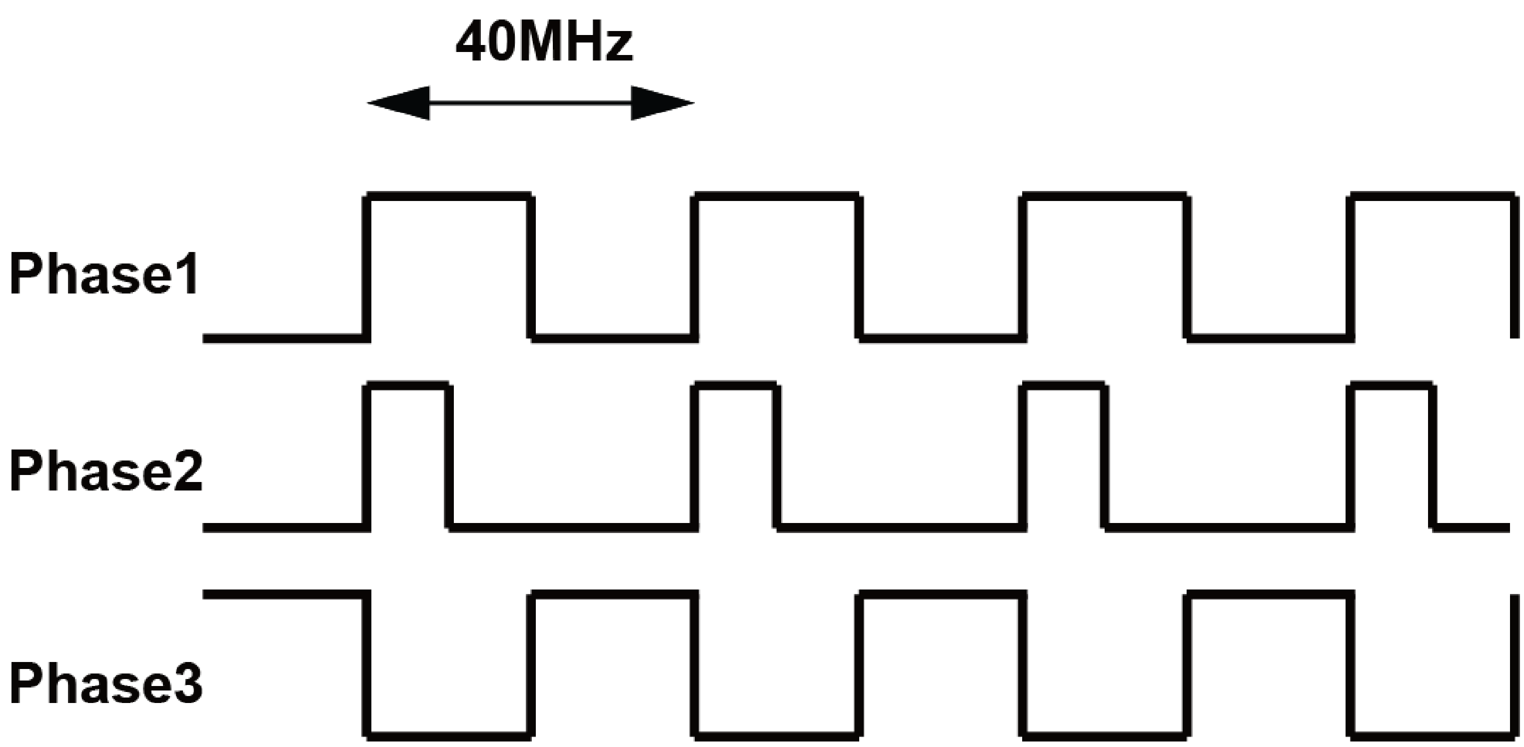
schedule



	Now~2/26	2/26~3/26	3/26~4/26
Layout	Stage1 OPAMP	Stage 2 Clk buffer	Whole Chip
verification	presim(ADC) Stage1	stage2 with stage1	Whole Chip

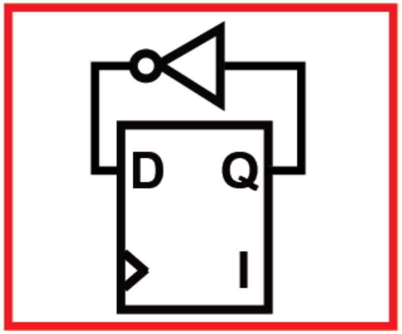
Clock Buffer

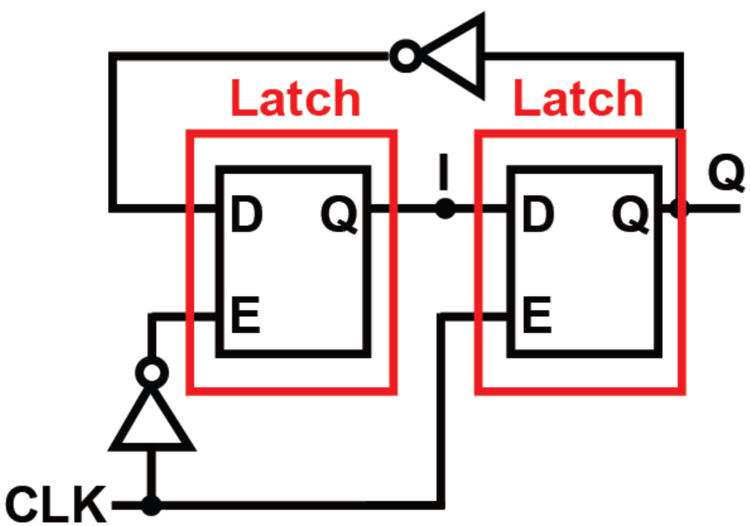
- In this ADC, three kinds of clock are used.

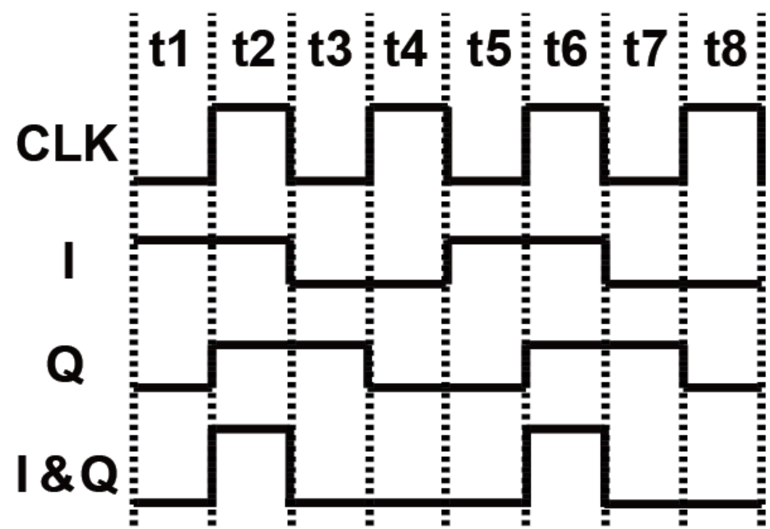


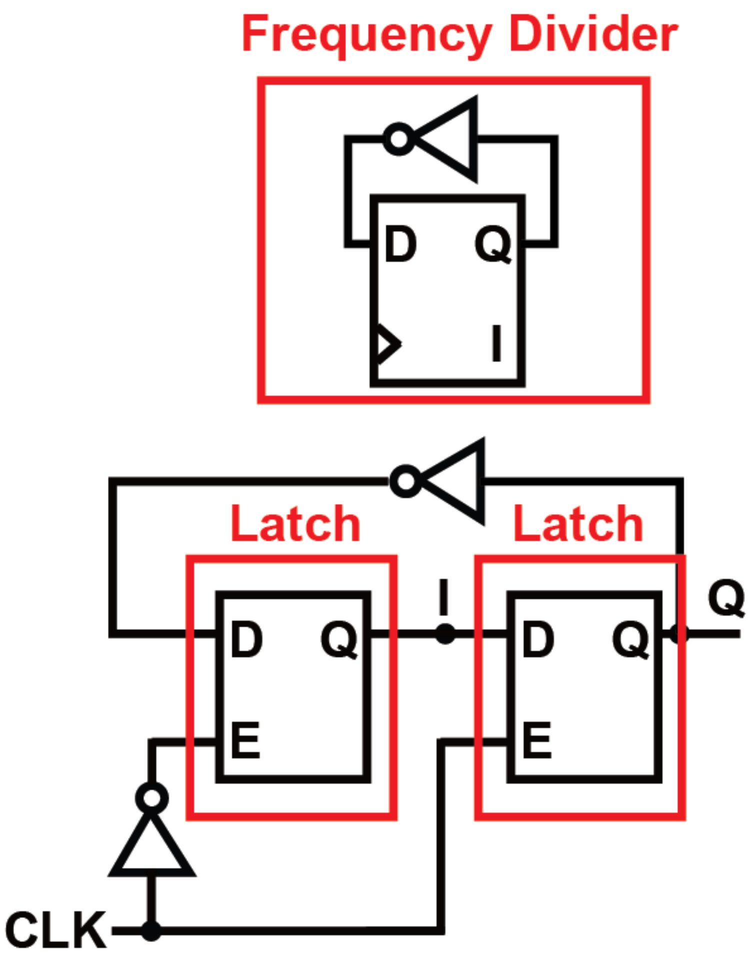
Clock Buffer

Frequency Divider

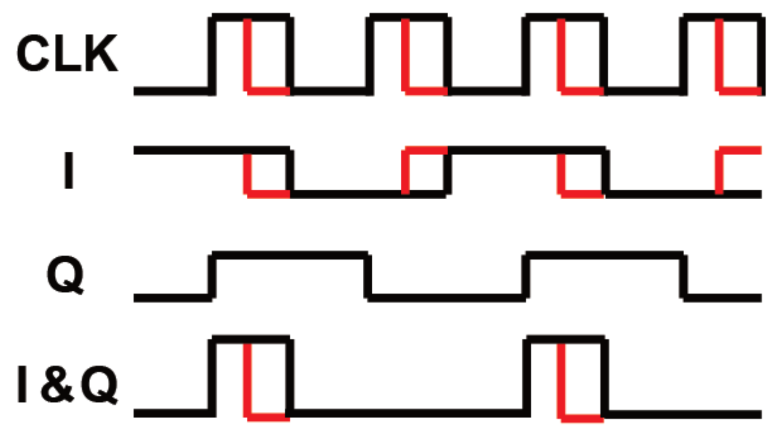




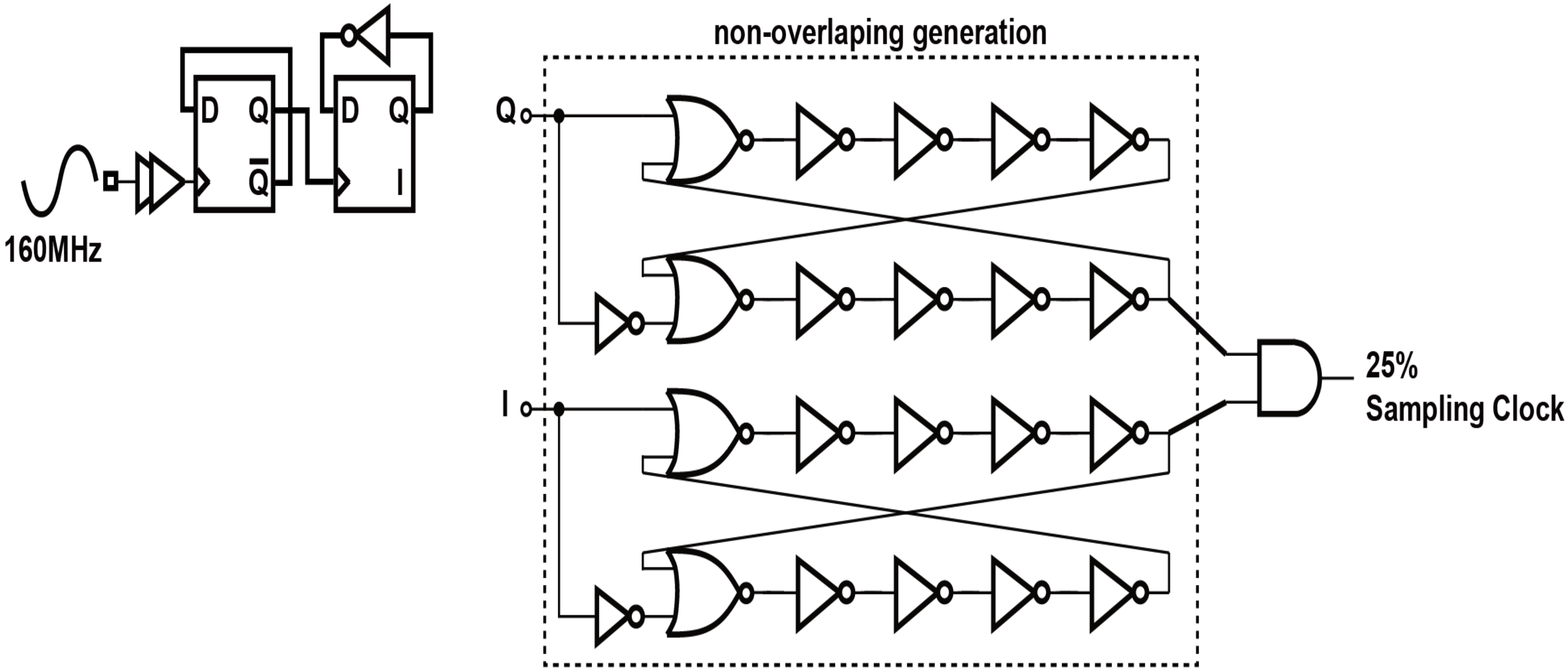




Frequency Divider
D
Q
I
Latch
Latch
D
Q
E
I
D
Q
E
Q
CLK

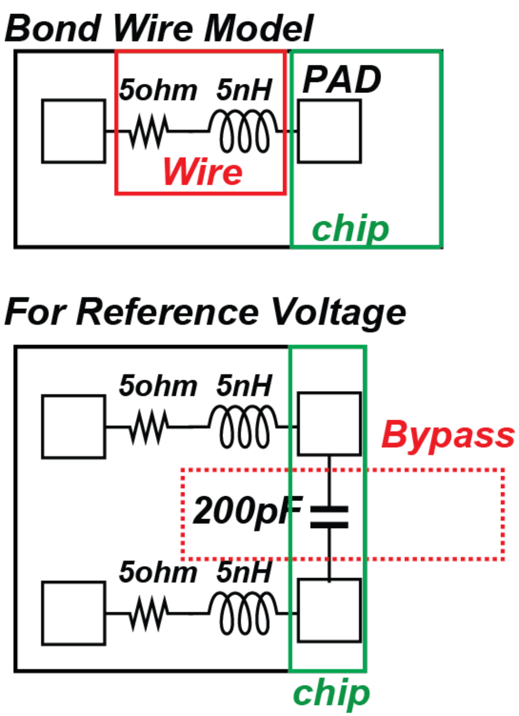


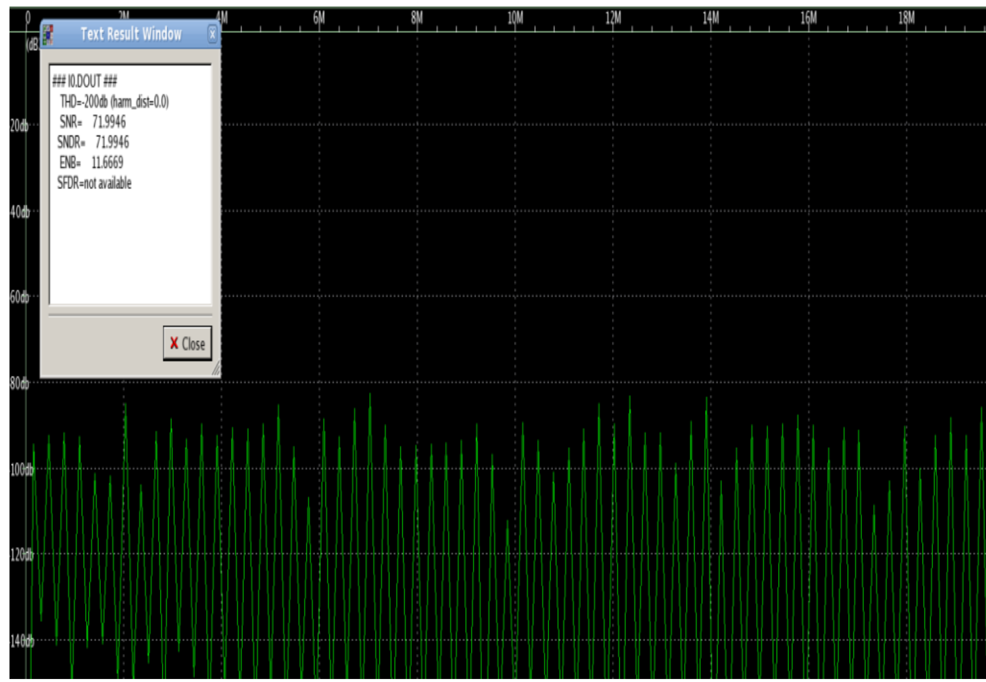
CLK
I
Q
I & Q



160MHz
D
Q
Q̄
D
Q
I
non-overlaping generation
Q
I
25%
Sampling Clock

Bonding wire simulation





Tapeout date?

Gustaff	John	Estimated Chip Back
	February 01	
February 15		
	February 22	
	April 05	
	April 26	July 12
May 25	May 25	August 16

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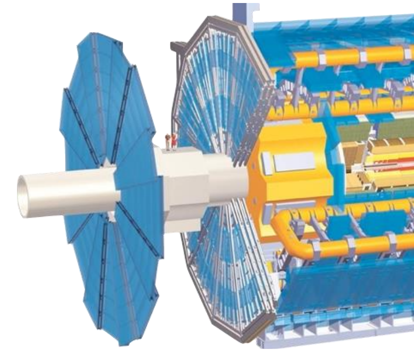


UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

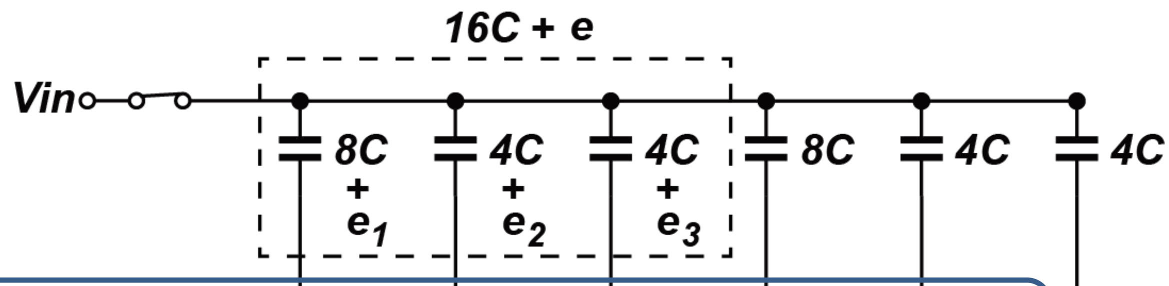
Chen-Kai Hsu

ckhsu@utexas.edu

Dec 20, 2016

Switching back

- Digital Sequence : 100



w	RS :	0	0	-vref	0	0
wo	RS :	-vref	-vref	-vref	+vref	+vref

After digitizing
Voltage @ bottom

Voltage @ Top plate

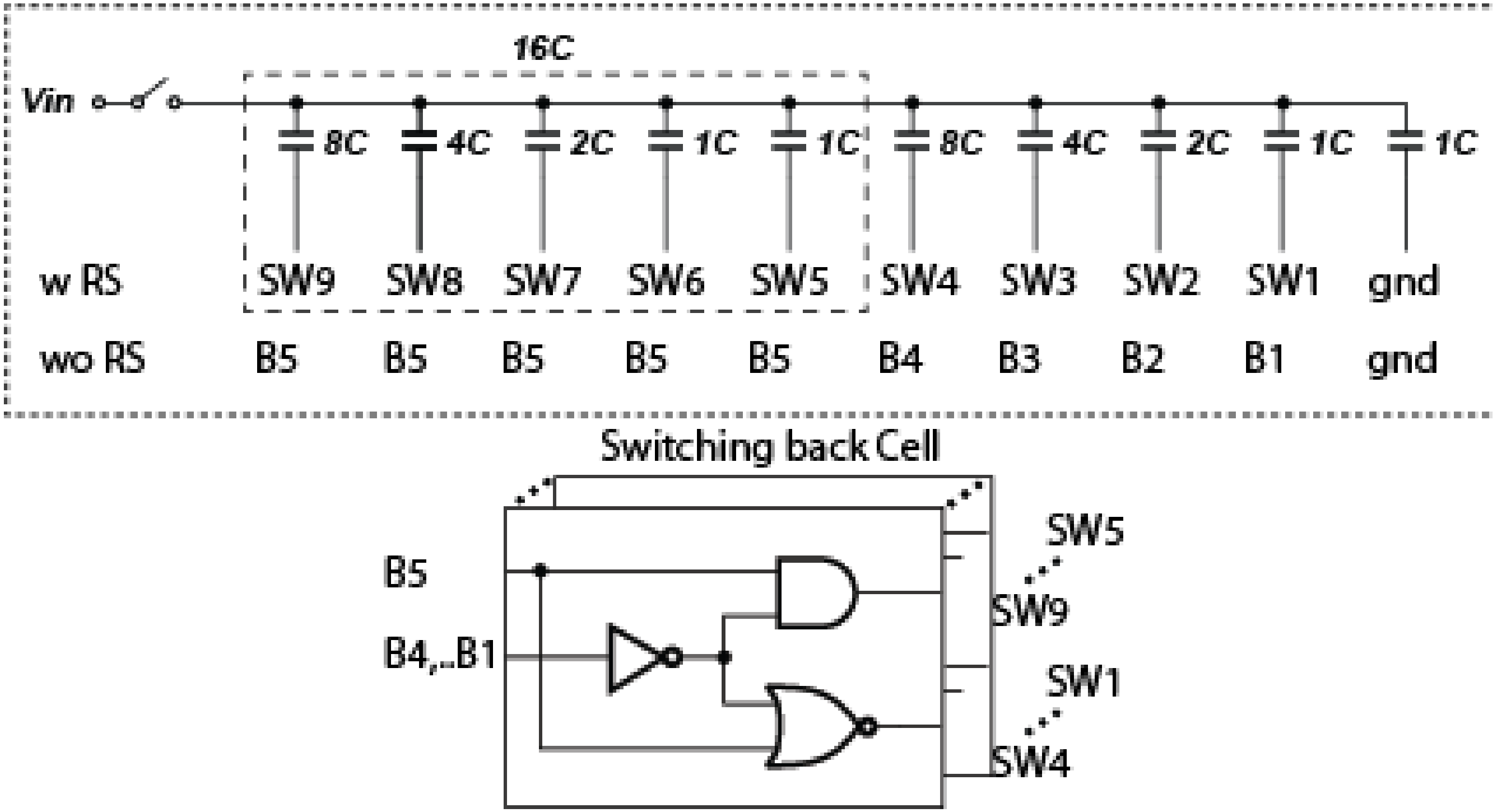
w RS : $Vin-((16c+e)/(32c+e))*vref+((8c+e1)/(32c+e))*vref+((4c+e2)/(32c+e))*vref$

wo RS : $Vin-((16c+e)/(32c+e))*vref+((8c)/(32c+e))*vref+((4c)/(32c+e))*vref$

- Remember that e equals to e1+e2+e3

Switching back(cont.)

- B5 controls SW9, SW8… SW5 if without switching back.



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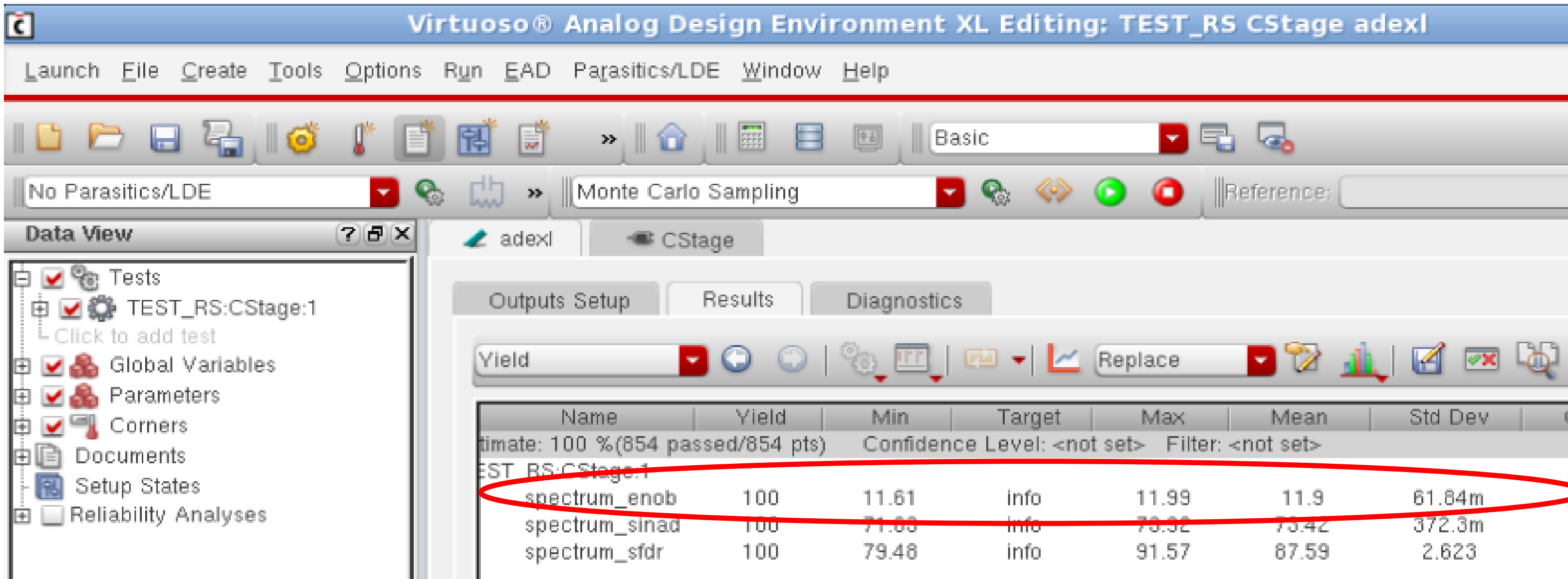
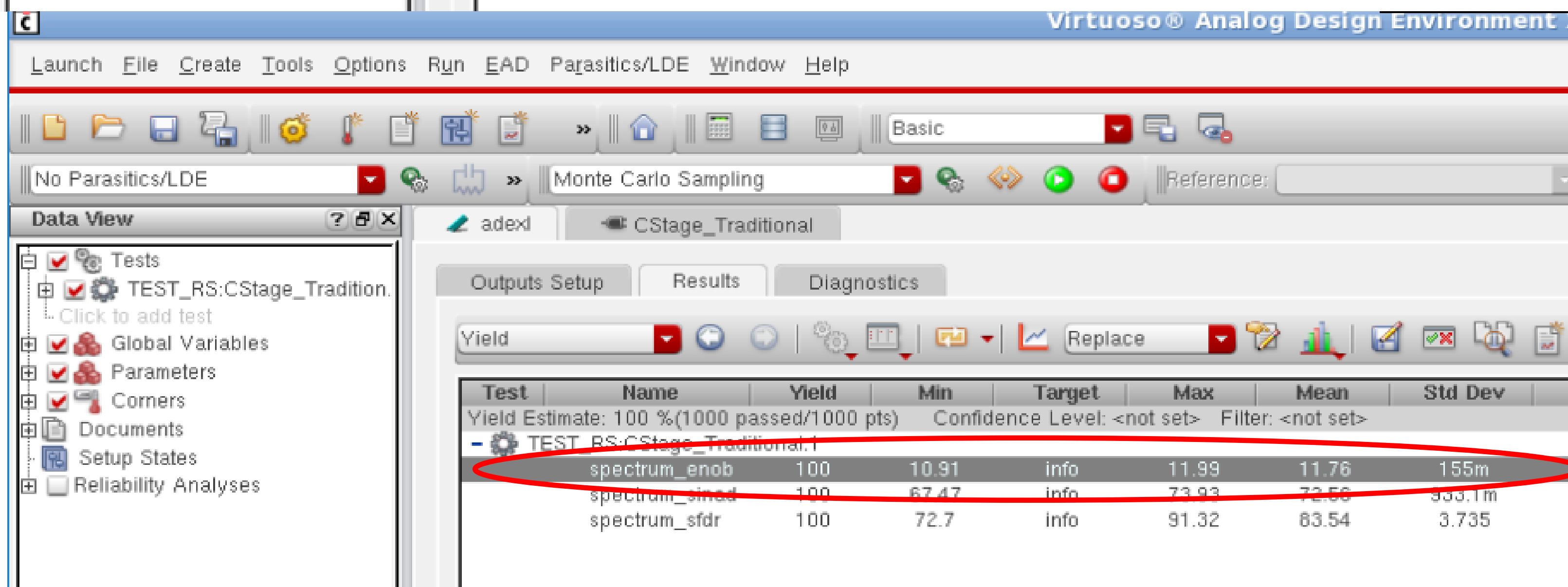
ATLAS EXPERIMENT

Simulation Result

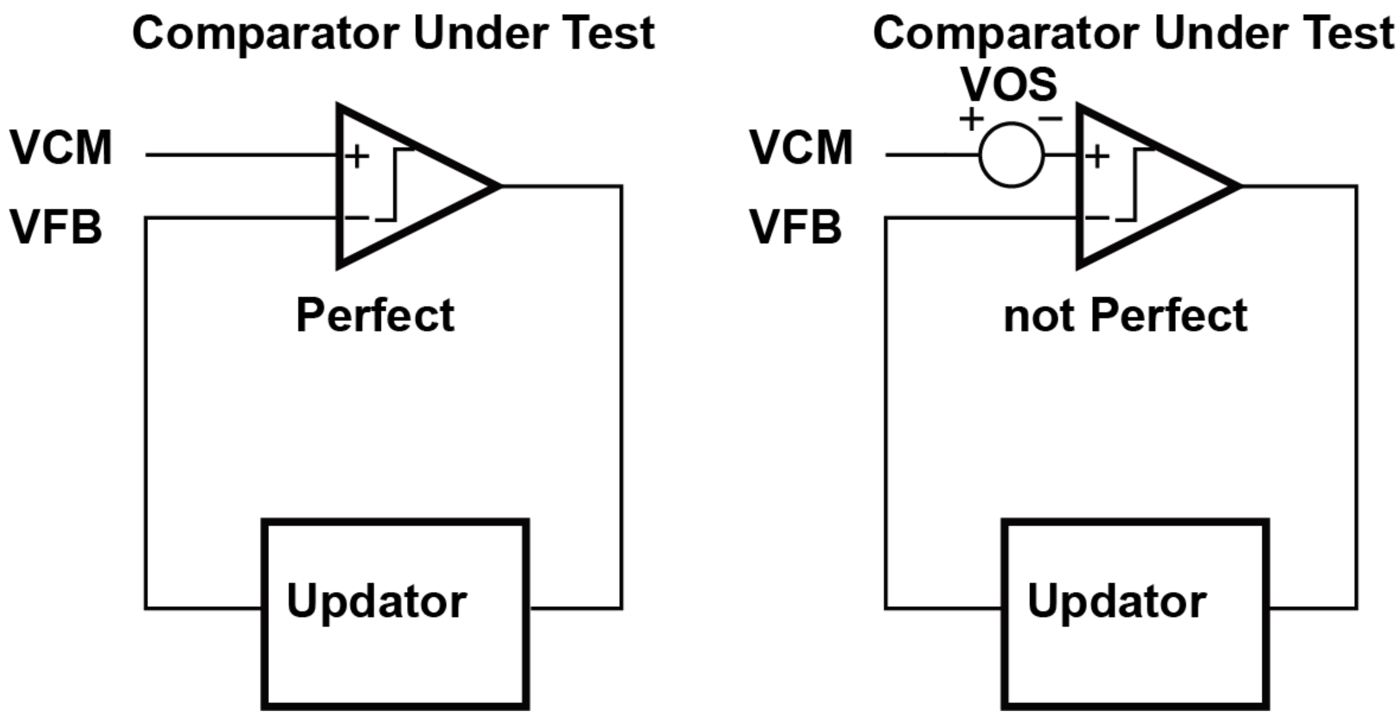
With Reverse switching



Without Reverse switching



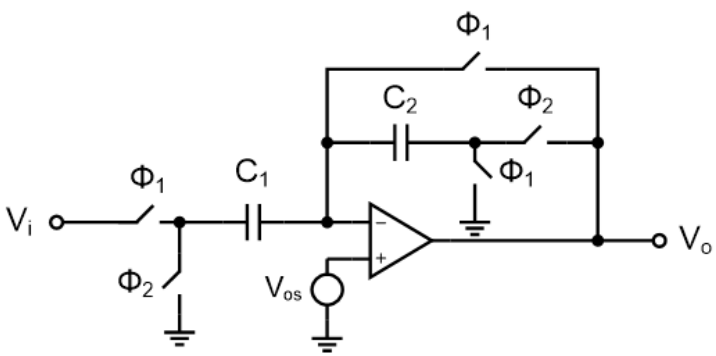
Comparator Offset Simulation



Test	Name	Yield	Min	Target	Max	Mean	Std Dev	C
Yield Estimate: 100 %(1000 passed/1000 pts)				Confidence Level: <not set>		Filter: <not set>		
ADC65LP:CLatchOffsetSimulTION:1								
	VOS	100	-15.63m	info	14.31m	326.8u	4.644m	

amplifier offset consideration

- Opamp offset canceled out by auto-zero technique.



$$\sum Q(\varphi_1) = [V_i(n) - V_{os}]C_1 - V_{os}C_2 \quad (1)$$

$$\sum Q(\varphi_2) = -V_{os}C_1 + [V_o(n) - V_{os}]C_2 \quad (2)$$

$$\boxed{H(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2}}$$

OPAMP Corner

- Most of corners meet our requirement.

Parameter	C0_0	C0_1	C0_2	C0_3	C0_4	C0_5	C0_6	C0_7
Model Group	TT	TT	TT	TT	TT	TT	TT	TT
VDD	1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32
temperature	-20	27	80	-20	27	80	-20	27

Output	C0_0	C0_1	C0_2	C0_3	C0_4	C0_5	C0_6	C0_7
gbw	3.291G	2.83G	2.425G	3.408G	3.015G	2.643G	3.53G	3.151G
gain	81.96	81.32	75.74	90.93	88	82.83	93.39	88.32

Parameter	C0_27	C0_28	C0_29	C0_30	C0_31	C0_32	C0_33	C0_34	C0_35
Model Group	FS	FS	FS	FS	FS	FS	FS	FS	FS
VDD	1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
temperature	-20	27	80	-20	27	80	-20	27	80

1.08
Parameter: VDD

Output	C0_27	C0_28	C0_29	C0_30	C0_31	C0_32	C0_33	C0_34	C0_35
gbw	3.12G	2.769G	2.274G	3.427G	2.921G	2.5G	3.501G	3.055G	2.658G
gain	33.79	81.93	72.95	88.2	85.28	79.84	90.86	85.73	81.03

Parameter	C0_18	C0_19	C0_20	C0_21	C0_22	C0_23	C0_24	C0_25	C0_26
Model Group	SS	SS	SS	SS	SS	SS	SS	SS	SS
VDD	1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
temperature	-20	27	80	-20	27	80	-20	27	80

Output	C0_18	C0_19	C0_20	C0_21	C0_22	C0_23	C0_24	C0_25	C0_26
gbw	3.084G	2.878G	2.329G	3.055G	.023G	2.604G	3.213G	3.147G	2.742G
gain	33.75	81.55	76.65	53.99	90.9	85.98	61.82	92.34	86.83

Parameter	C0_36	C0_37	C0_38	C0_39	C0_40	C0_41	C0_42	C0_43	C0_44
Model Group	SF	SF	SF	SF	SF	SF	SF	SF	SF
VDD	1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
temperature	-20	27	80	-20	27	80	-20	27	80

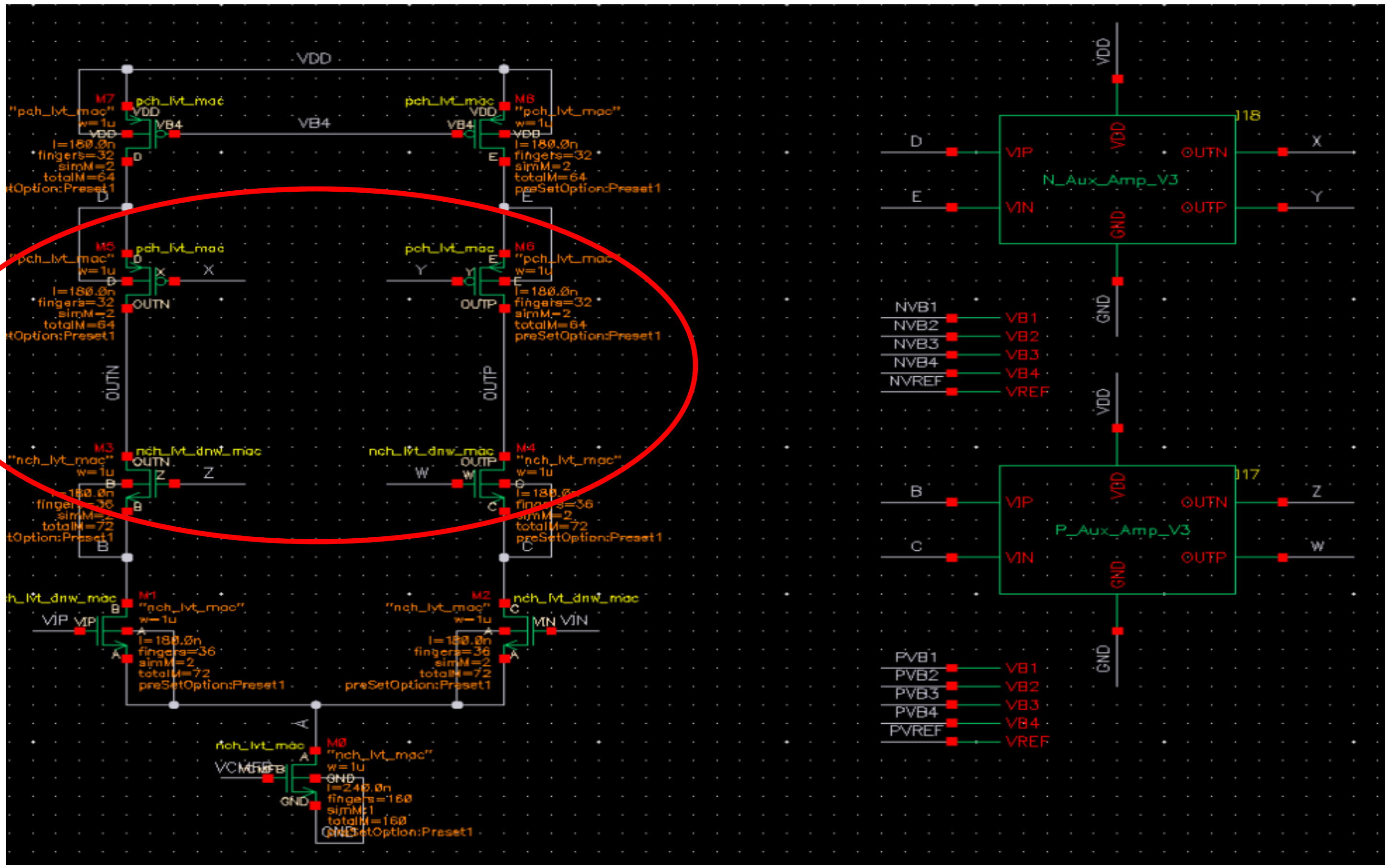
Output	C0_36	C0_37	C0_38	C0_39	C0_40	C0_41	C0_42	C0_43	C0_44
gbw	2.901G	2.904G	2.577G	3.016G	3.098G	2.763G	3.244G	3.24G	2.899G
gain	36.44	79.3	76.38	32.43	88.03	84.2	64.74	89.4	84.92

Parameter	C0_9	C0_10	C0_11	C0_12	C0_13	C0_14	C0_15	C0_16	C0_17
Model Group	FF	FF	FF	FF	FF	FF	FF	FF	FF
VDD	1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
temperature	-20	27	80	-20	27	80	-20	27	80

Output	C0_9	C0_10	C0_11	C0_12	C0_13	C0_14	C0_15	C0_16	C0_17
gbw	3.226G	2.835G	2.482G	3.395G	3.026G	2.675G	3.535G	3.175G	2.823G
gain	83.5	79.3	70.98	88.59	83.34	77.66	88.83	84.09	78.85

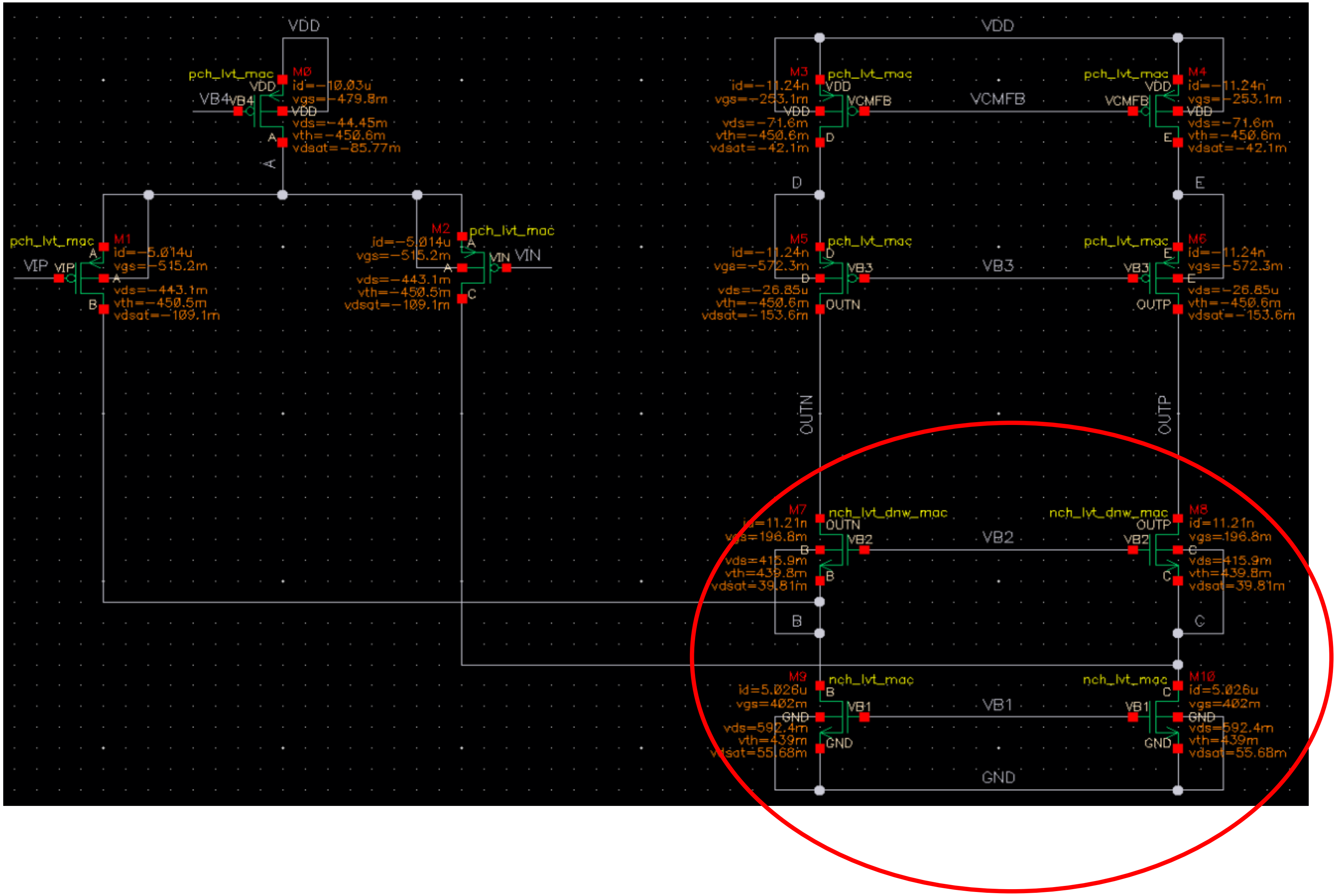
OPAMP Corner

- N_Aux_Amp: N mos input folded cascade
- P_Aux_Amp: P mos input folded cascode



OPAMP Corner

- P_Aux_Amp: P mos input folded cascode



Amplifier Corner simulation

C0_0	C0_1	C0_2	C0_3	C0_4	C0_5	C0_6	C0_7	C0_8
TT	TT	TT	TT	TT	TT	TT	TT	TT
1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
-20	27	80	-20	27	80	-20	27	80
2.363G	2.227G	2.121G	3.167G	2.897G	2.625G	3.698G	3.424G	3.139G
87.33	84.37	75.49	89.79	88.19	83.13	90.84	89.08	82.93

C0_36	C0_37	C0_38	C0_39	C0_40	C0_41	C0_42	C0_43	C0_44
SF	SF	SF	SF	SF	SF	SF	SF	SF
1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
-20	27	80	-20	27	80	-20	27	80
2.589G	2.334G	2.201G	3.296G	3.037G	2.77G	3.785G	3.521G	3.222G
87.84	82.56	73.57	90.19	87.52	78.32	91.06	88.55	77.07

C0_9	C0_10	C0_11	C0_12	C0_13	C0_14	C0_15	C0_16	C0_17
FF	FF	FF	FF	FF	FF	FF	FF	FF
1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
-20	27	80	-20	27	80	-20	27	80
2.584G	2.313G	2.19G	3.405G	3.129G	2.858G	3.894G	3.622G	3.344G
84.16	80.91	72.6	87.91	86.09	80.81	89.23	87.18	80.04

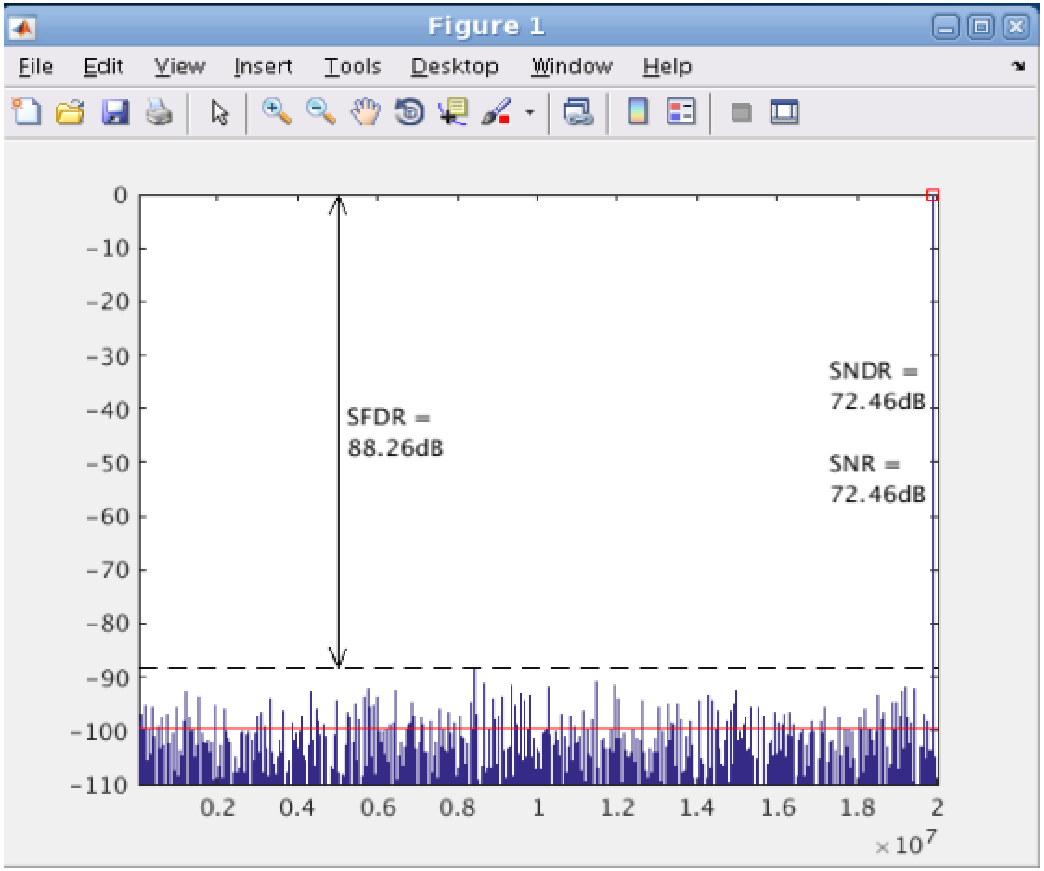
C0_27	C0_28	C0_29	C0_30	C0_31	C0_32	C0_33	C0_34	C0_35
FS	FS	FS	FS	FS	FS	FS	FS	FS
1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
-20	27	80	-20	27	80	-20	27	80
2.053G	2.022G	1.955G	2.972G	2.71G	2.45G	3.6G	3.321G	3.047G
81.32	80.76	74.1	87.78	86.88	83.62	89.97	88.65	84.98

C0_18	C0_19	C0_20	C0_21	C0_22	C0_23	C0_24	C0_25	C0_26
SS	SS	SS	SS	SS	SS	SS	SS	SS
1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
-20	27	80	-20	27	80	-20	27	80
2.193G	2.11G	2.012G	2.888G	2.618G	2.347G	3.479G	3.201G	2.914G
88.69	85.82	76.65	90.89	89.36	83.82	91.96	90.39	85.01

- 45 corner was tested.
- Temperature:{-20,27,80}
- MOS :{TT,SS,FF,SF,FS}
- VDD :0.9VDD,VDD,1.1VDD

TT, 27, 1.2V with transient noise

	Power Consumption
VDD	1.2V
Sample Rates	40MS/s
SNDR	72.46dB = 11.74 bits
Power Consumption	3mW



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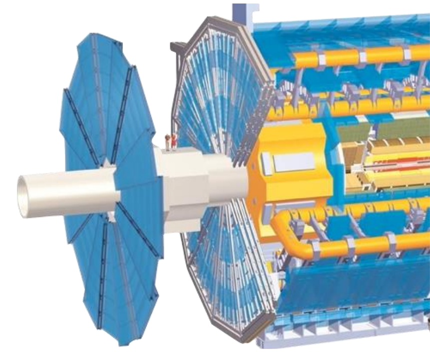
Future Work

- Corner simulation of whole 12-b ADC
- 12-b Pipeline SAR ADC simulation together with bonding wire.
- DAC Array layout.



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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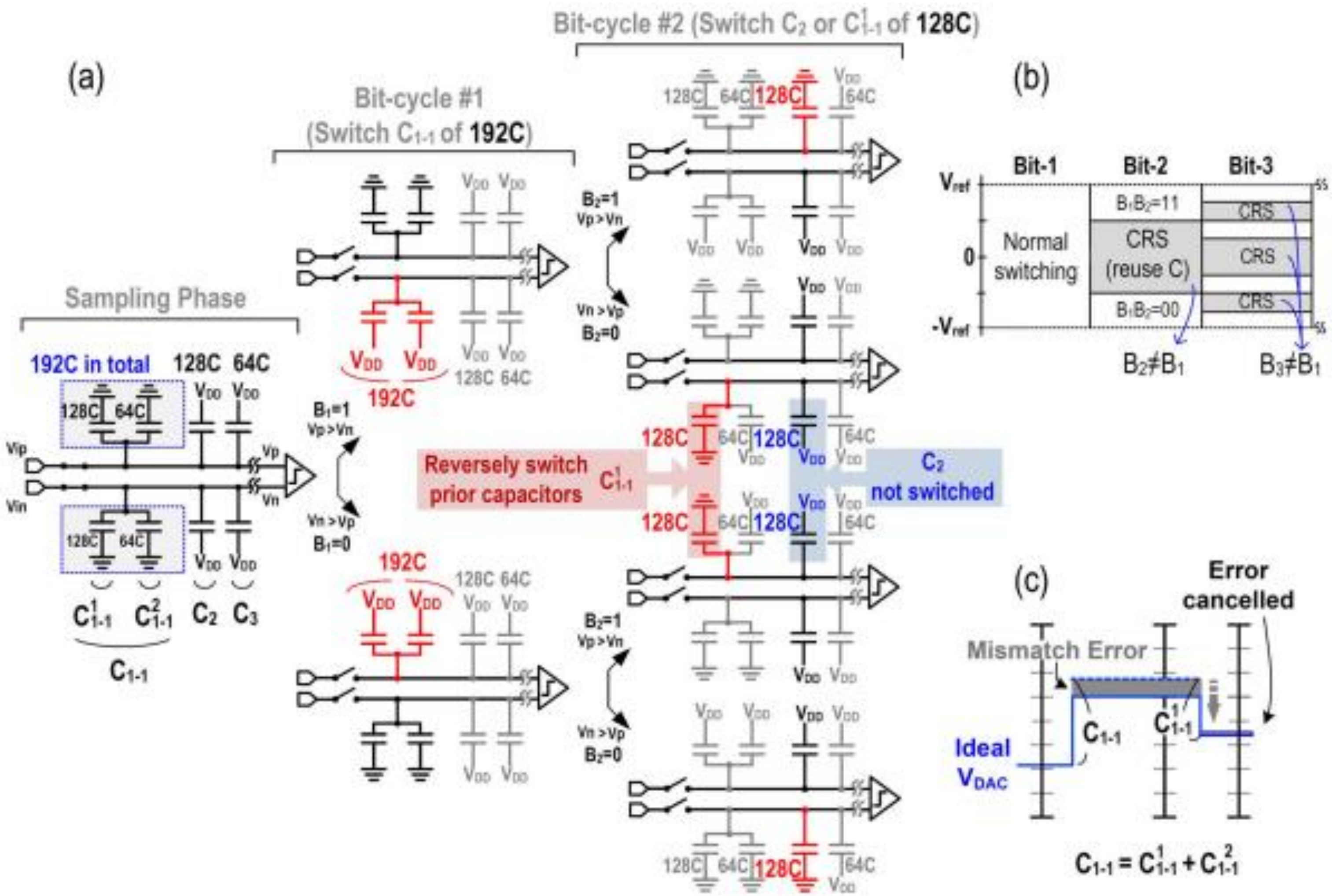
Nov 22, 2016

Outline

- Capacitor Linearity Enhancement
- Implementation Progress
- Future work

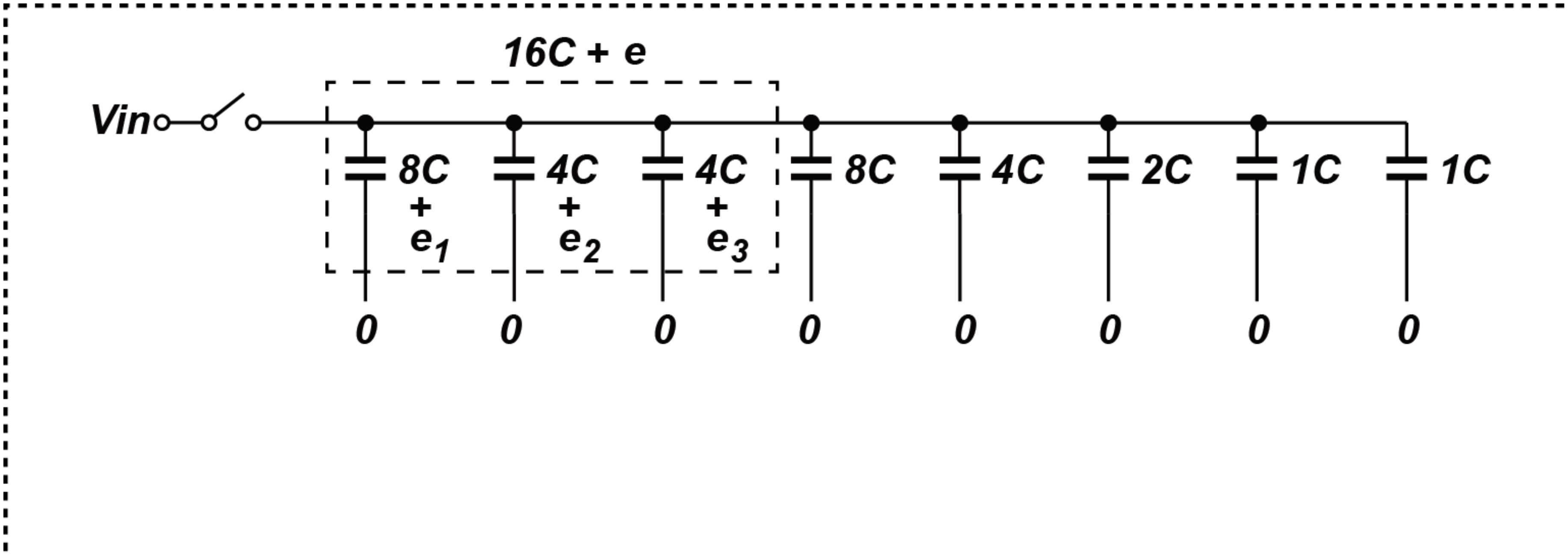
Capacitor Matching Enhancement

- Reversed Switching, RS, [1] JSSCC'15



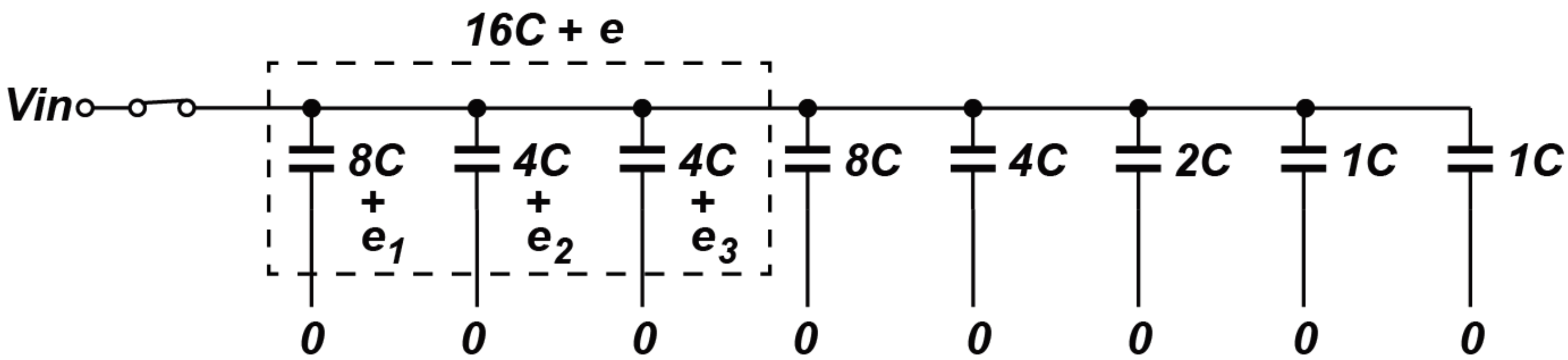
Capacitor Matching Enhancement

- Digital Sequence : 100



Capacitor Matching Enhancement

- Digital Sequence : 100



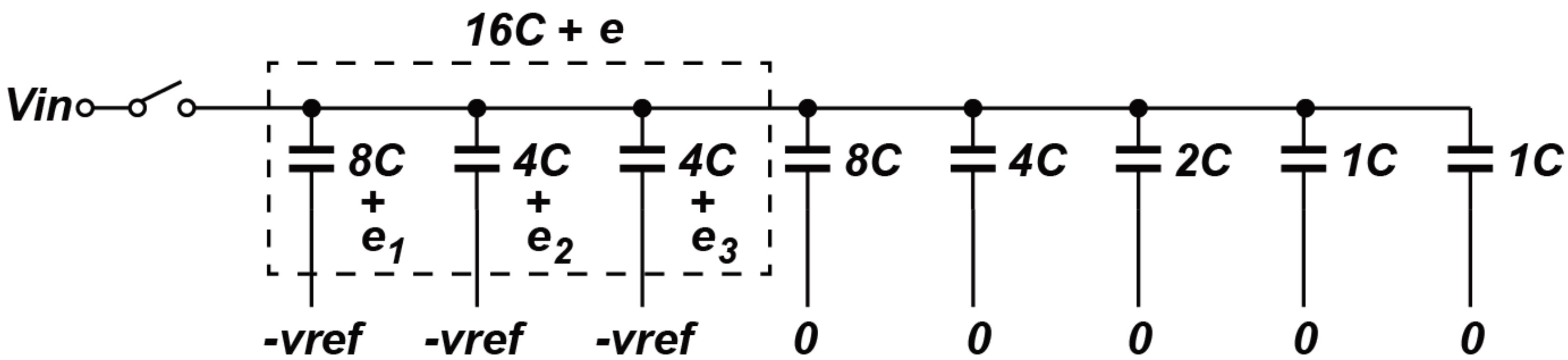
Voltage @ Top plate

w RS : Vin

wo RS : Vin

Capacitor Matching Enhancement

- Digital Sequence : 100



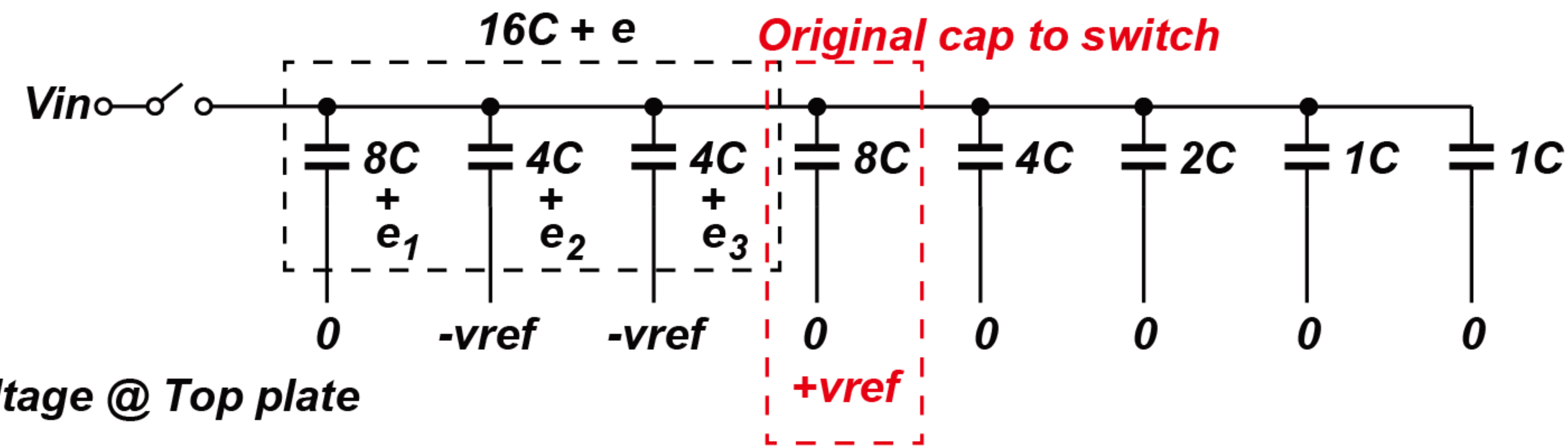
Voltage @ Top plate

*w RS : Vin-((16c+e)/(32c+e))*vref*

*wo RS : Vin-((16c+e)/(32c+e))*vref*

Capacitor Matching Enhancement

- Digital Sequence : 100



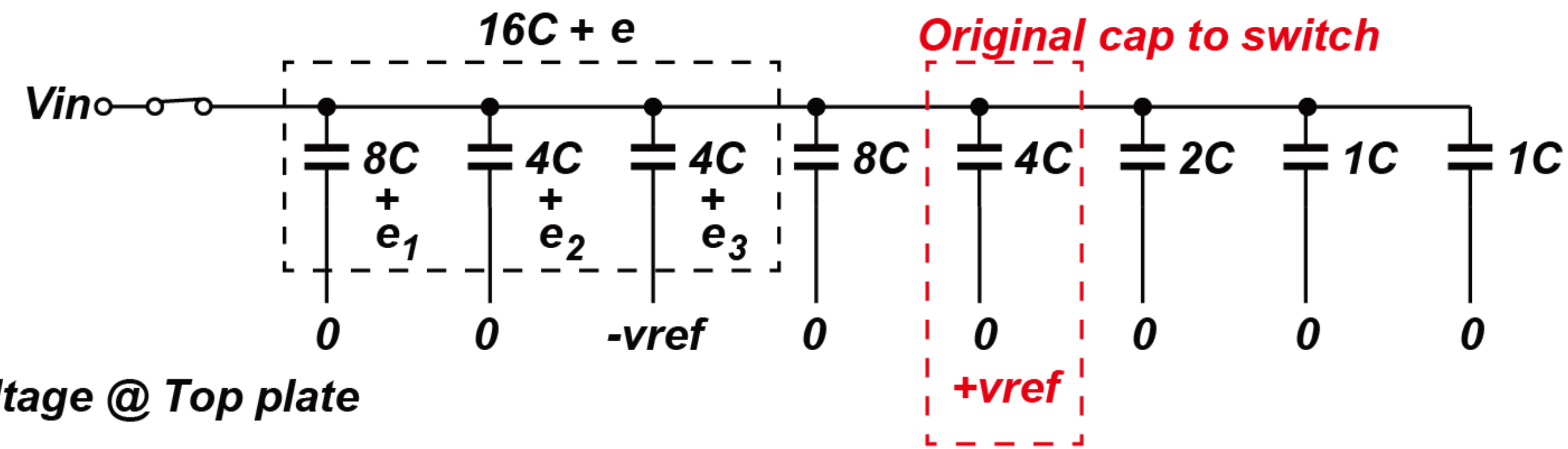
Voltage @ Top plate

w RS : $Vin-((16c+e)/(32c+e))*vref+((8c+e1)/(32c+e))*vref$

wo RS : $Vin-((16c+e)/(32c+e))*vref+((8c)/(32c+e))*vref$

Capacitor Matching Enhancement

- Digital Sequence : 100



Voltage @ Top plate

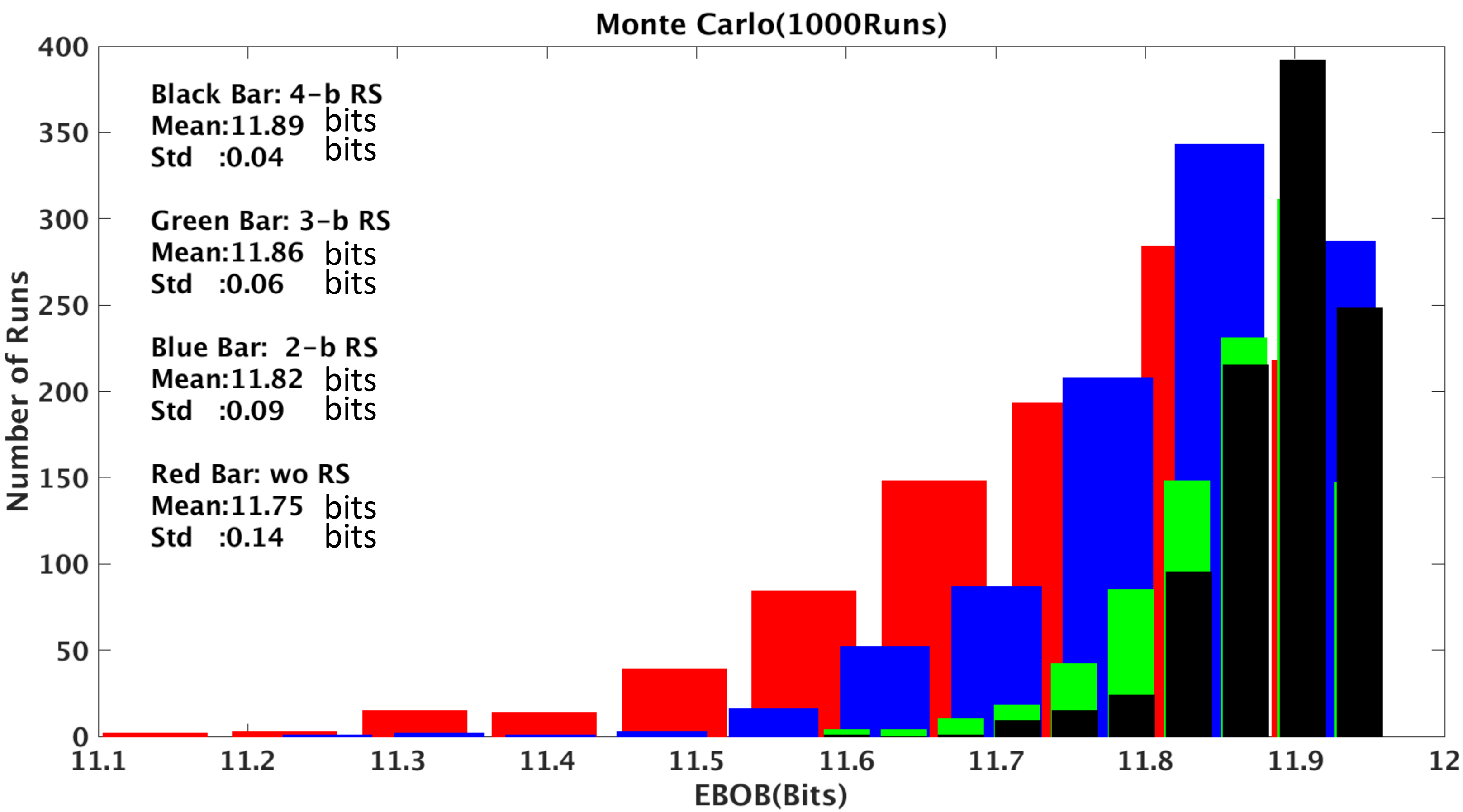
w RS : Vin-((16c+e)/(32c+e))*vref+((8c+e1)/(32c+e))*vref+((4c+e2)/(32c+e))*vref

wo RS : Vin-((16c+e)/(32c+e))*vref+((8c)/(32c+e))*vref+((4c)/(32c+e))*vref

- Remember that e equals to e1+e2+e3

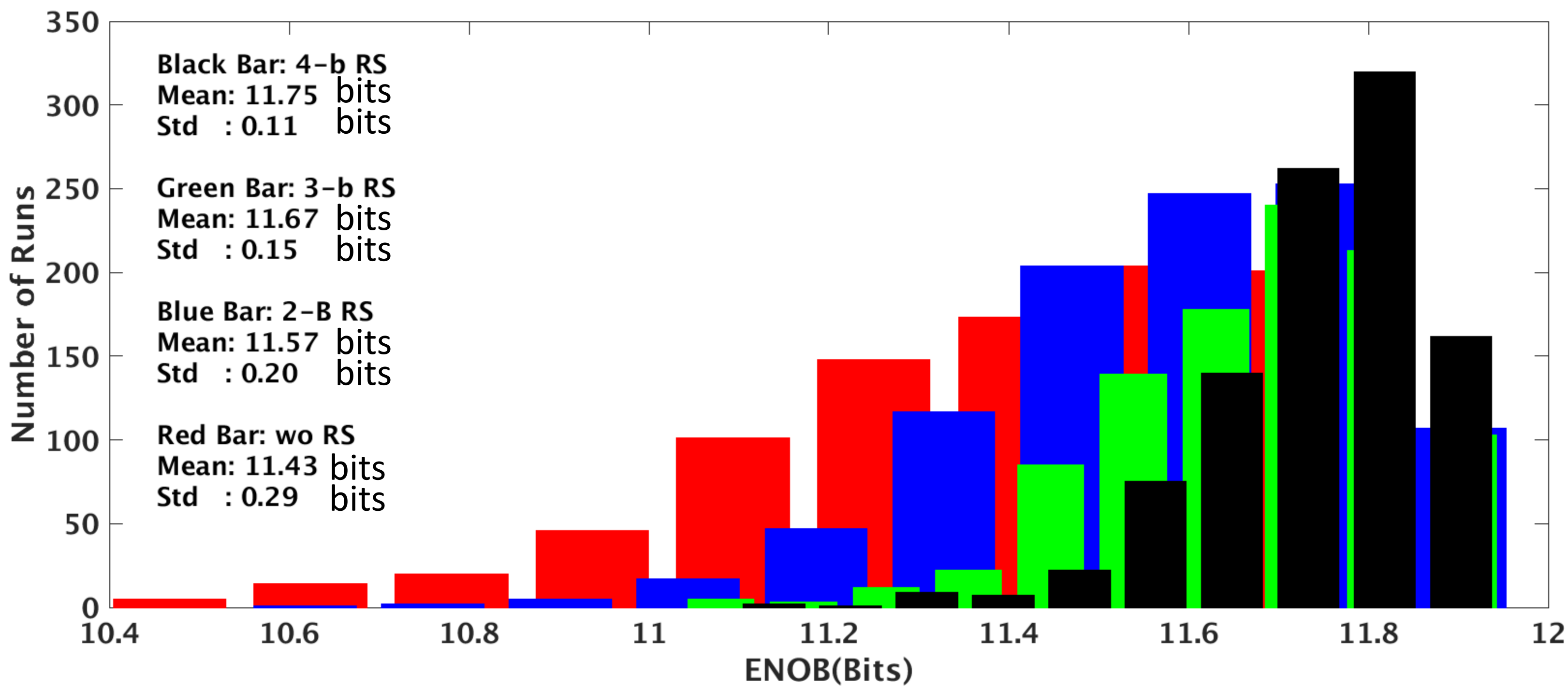
Capacitor Matching Enhancement

- Unit capacitor of 200fF in 1st stage.



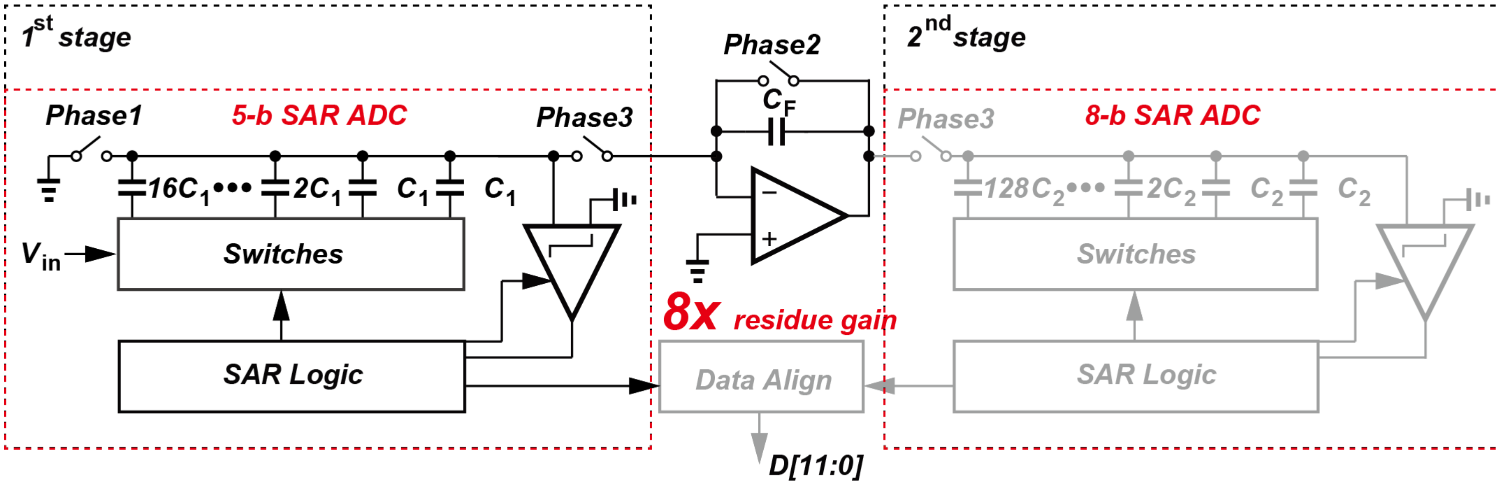
Capacitor Matching Enhancement

- Unit capacitor of 20fF in 1st stage.



Implementation Progress

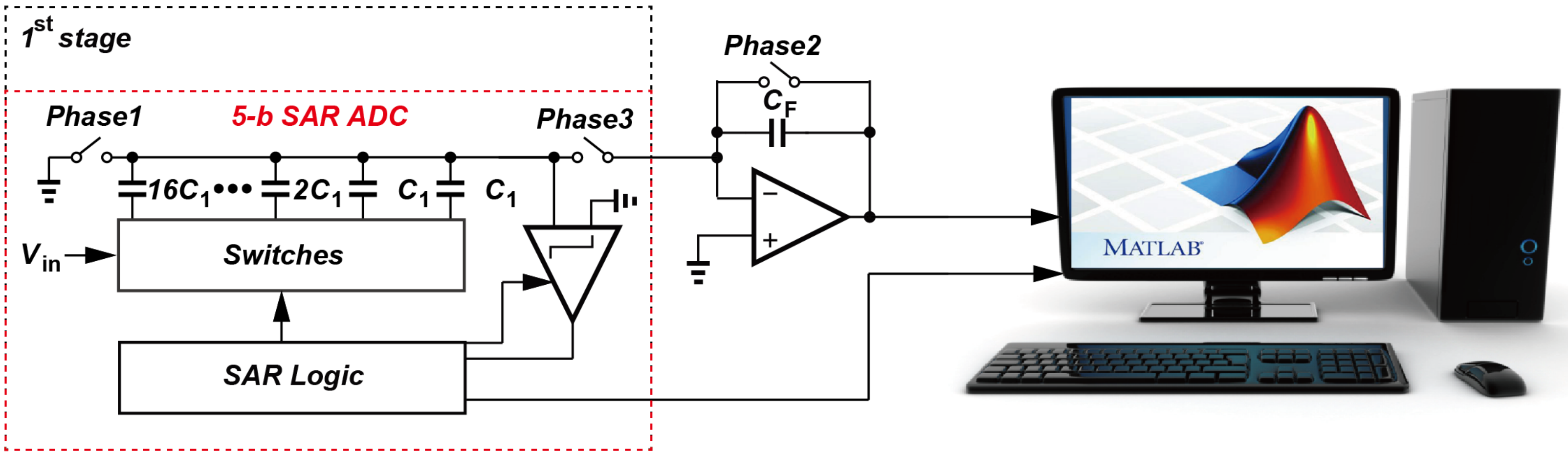
- First stage has been built(without RS).

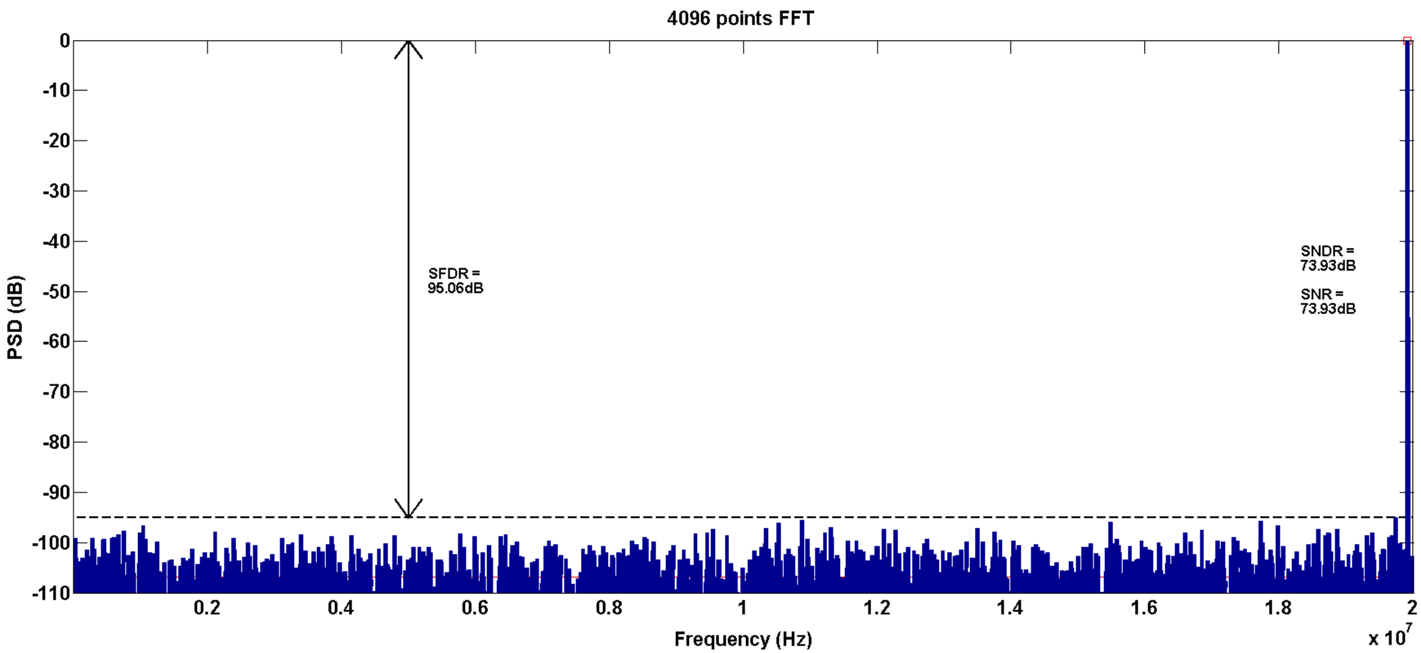


	Power Consumption
OPAMP	1.8mW
1st Comparator	60uW
1st SAR Logic	20uW
Bootstrap Switch	6uW

Implementation Progress

- Feed the residue of amplifier and digital code into Matlab.





Future Work

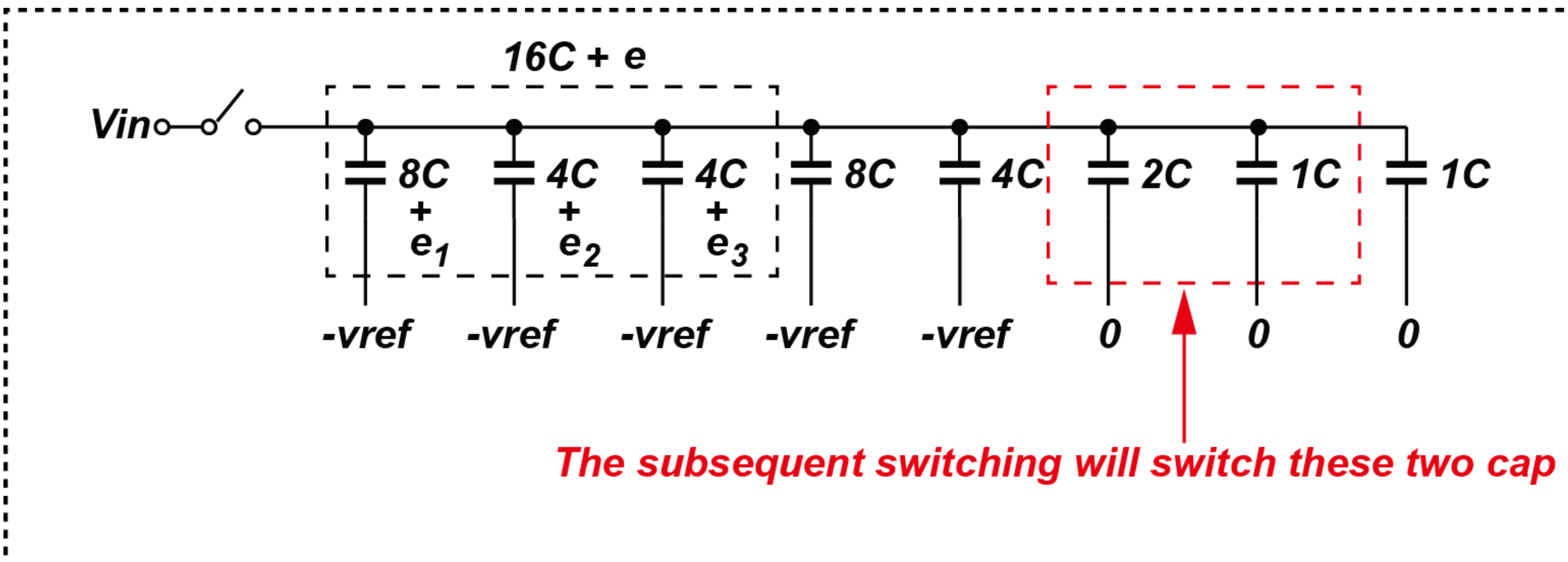
- Implement the RS technique into the first stage.
- Doing more simulation on first stage before next meeting, such as corner simulation and noise simulation.

Reference

1. J.-H. Tsai et al., "A 0.003 mm2 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS with digital error correction and correlated-reversed switching," IEEE J. Solid-State Circuits, vol. 50, no. 6, pp. 1382–1398, Jun. 2015.

Backup

If the digitized code is 111, the following switching will not switch back.

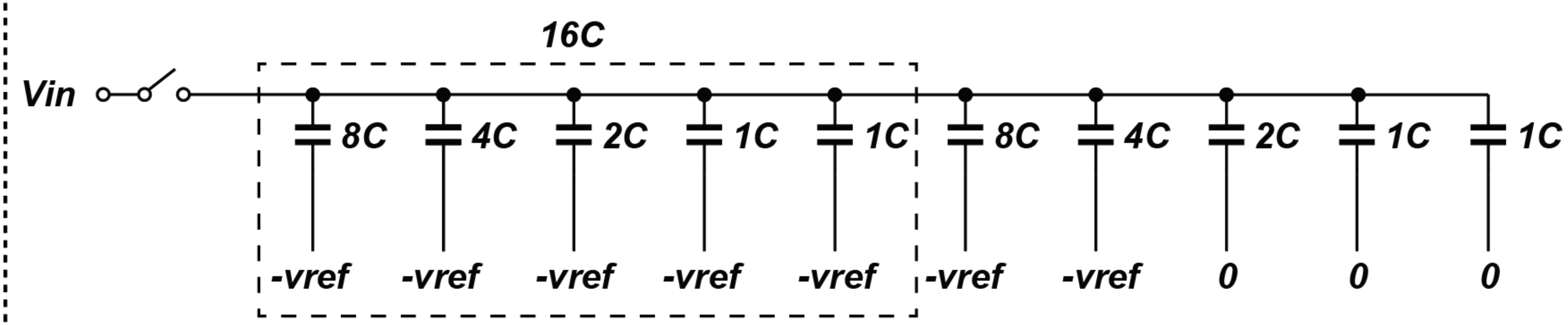


Backup

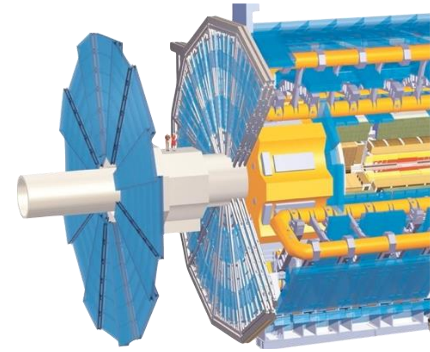
Performing more bits RS will alleviate this dilemma.

Assuming 111 has been resolved and the following sequence will be 00, 01, 10, 11.

Except for 11111, the other sequence will have at least one switching back.



11100	-vref	-vref	0	0	-vref	-vref	-vref	0	0	0
11101	-vref	-vref	0	-vref	-vref	-vref	-vref	0	-vref	0
11110	-vref	-vref	-vref	0	-vref	-vref	-vref	-vref	0	0
11111	-vref	-vref	-vref	-vref	-vref	-vref	-vref	-vref	-vref	0



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

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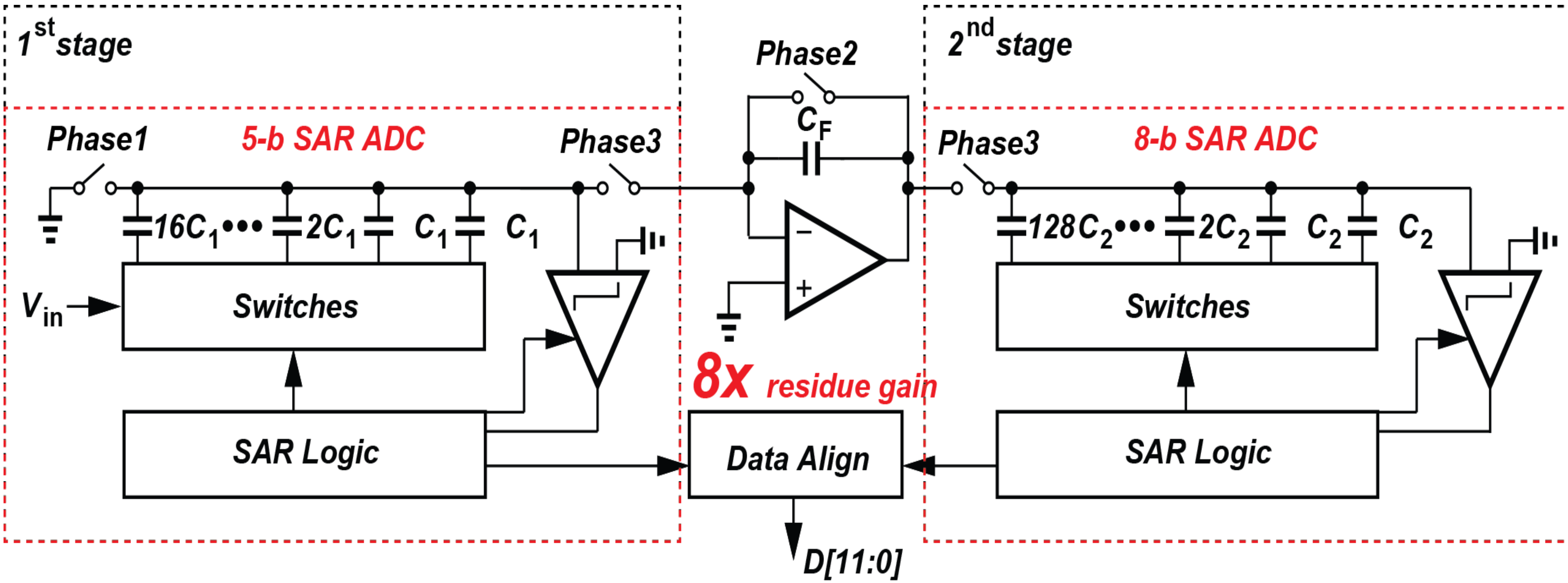
Nov 4, 2016

What about 8x inter-stage gain ?

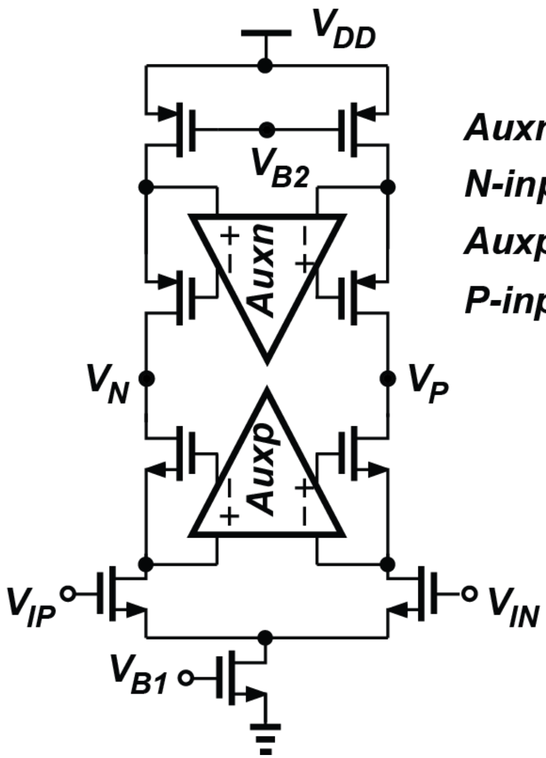


Open-Loop Gain can be reduced from 78dB to 72dB.

Unit-Gain Bandwidth can be reduced from 1.27GHz to 635MHz.

Due to reduced swing, maybe we can just use telescopic with gain boosting(One-stage which means low power).

OPAMP



Auxn:

N-input Folded Cascode

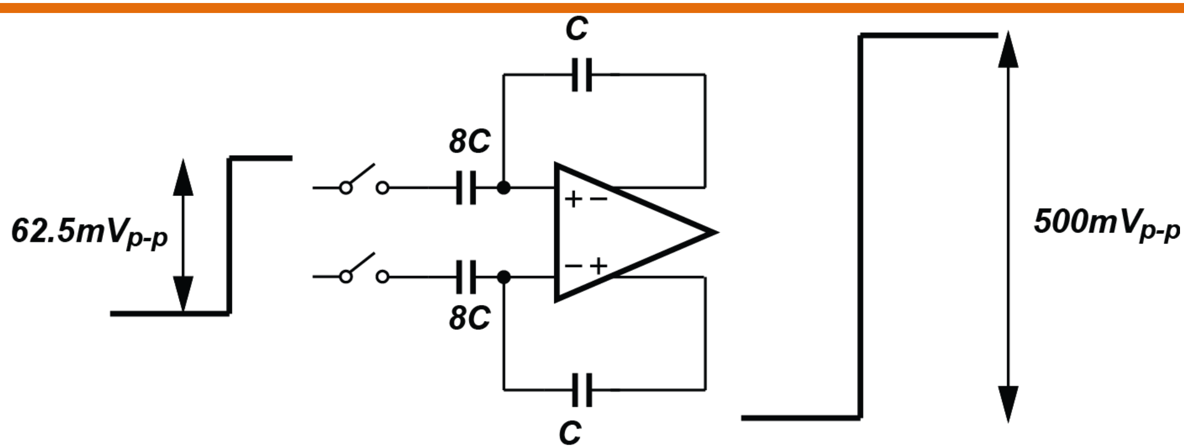
Auxp:

P-input Folded Cascode

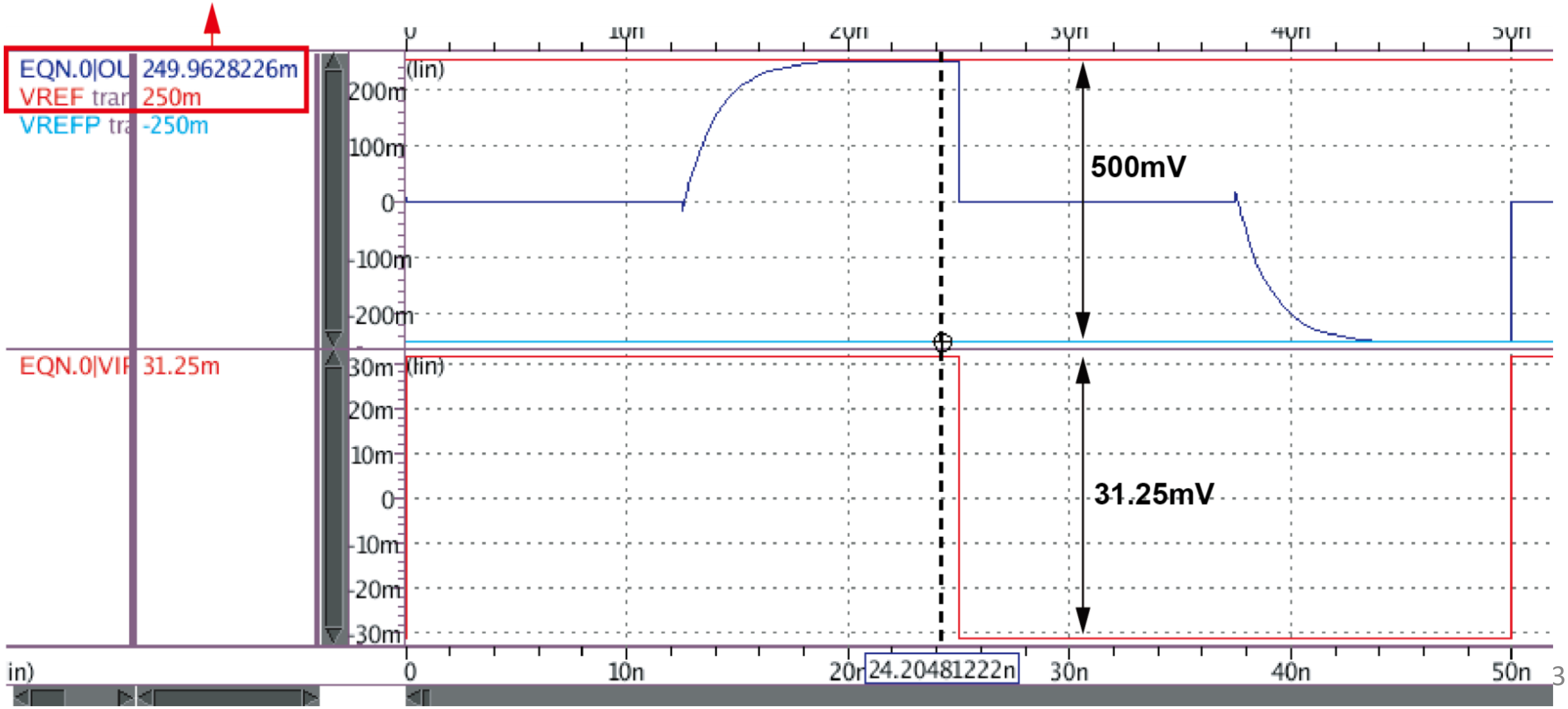
	Specification
Supply Voltage	1.2 V
Technology	TSMC 65LP 1P6M
DC Gain	80dB
Current-Main	750uA
Current-Auxn	100uA
Current-Auxp	100uA
Bias Circuit	200uA
PhaseMargin	80 degree
Unit-Gain Freq	2.1GHz

- According to [1], the frequency response of this opamp has to be carefully designed to ensure stability and to avoid pole-zero doublet, causing slow settling.
- $\beta\omega_{main,ta} < \omega_{aux,ta} < \omega_{main,2n\,pole}$

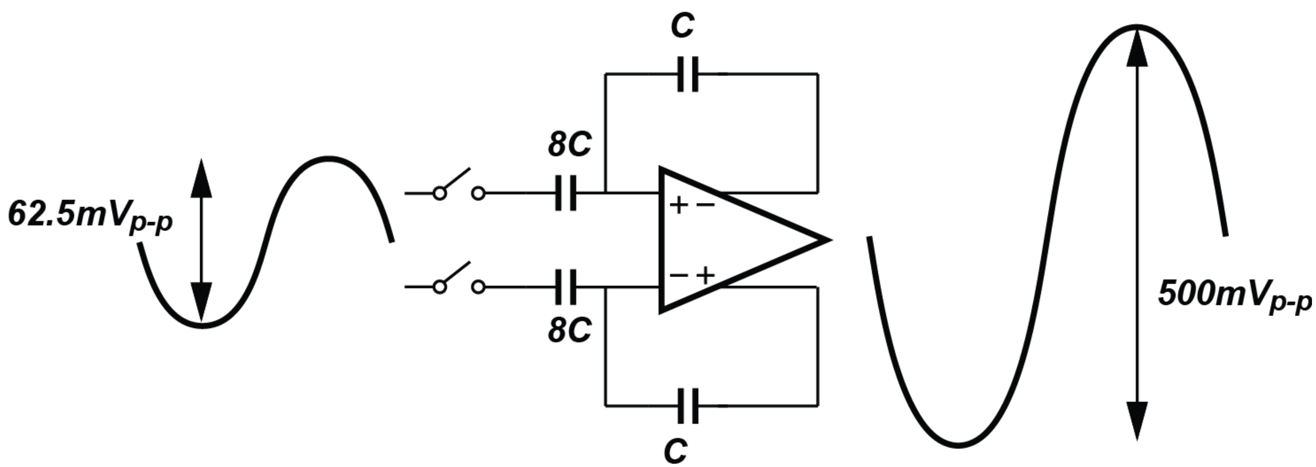
Step Response

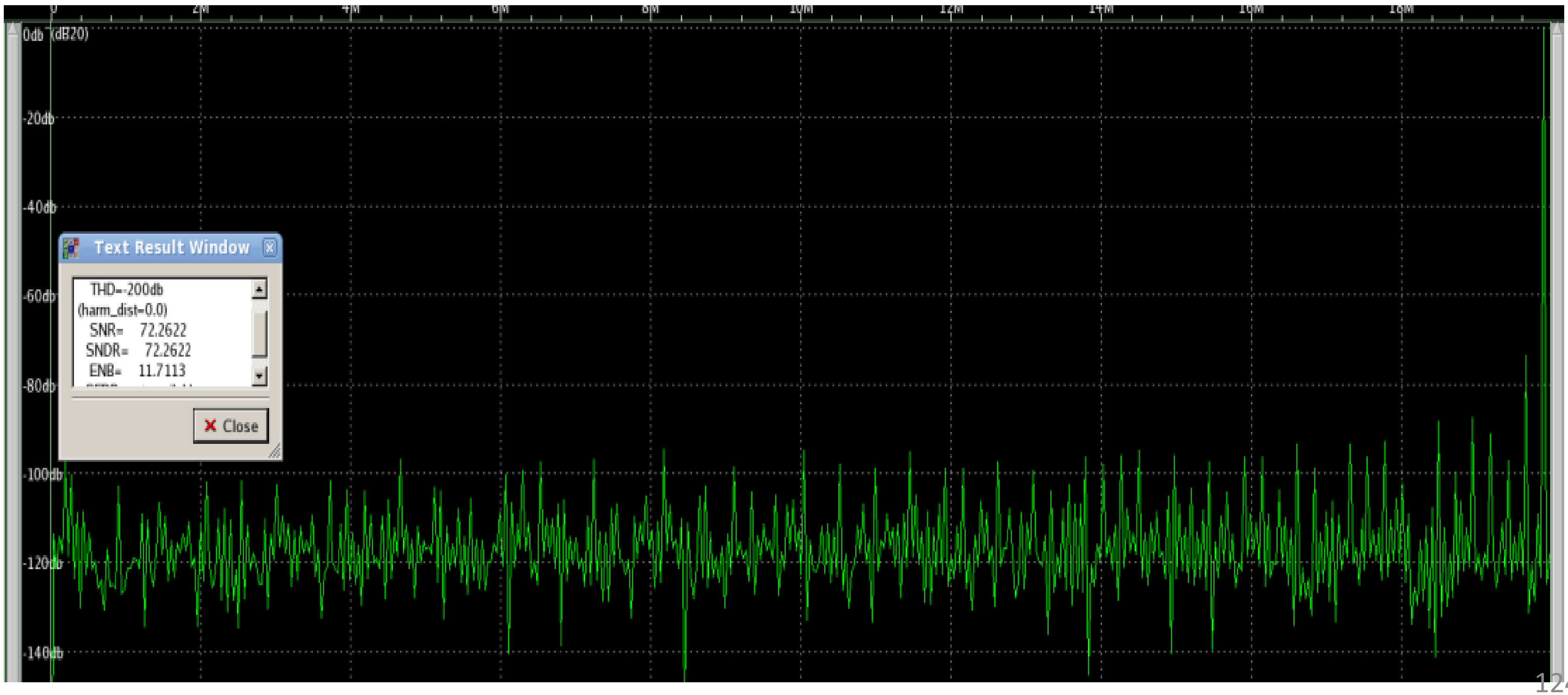


Error = 250m-249.96m = 0.04m < (0.5)/2^9



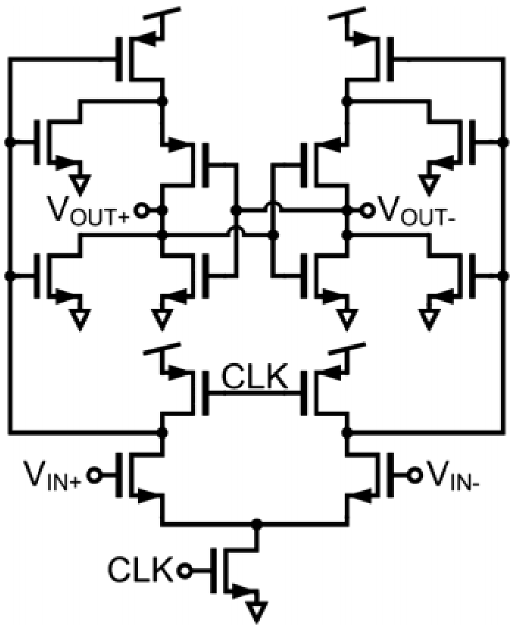
Linearity Test



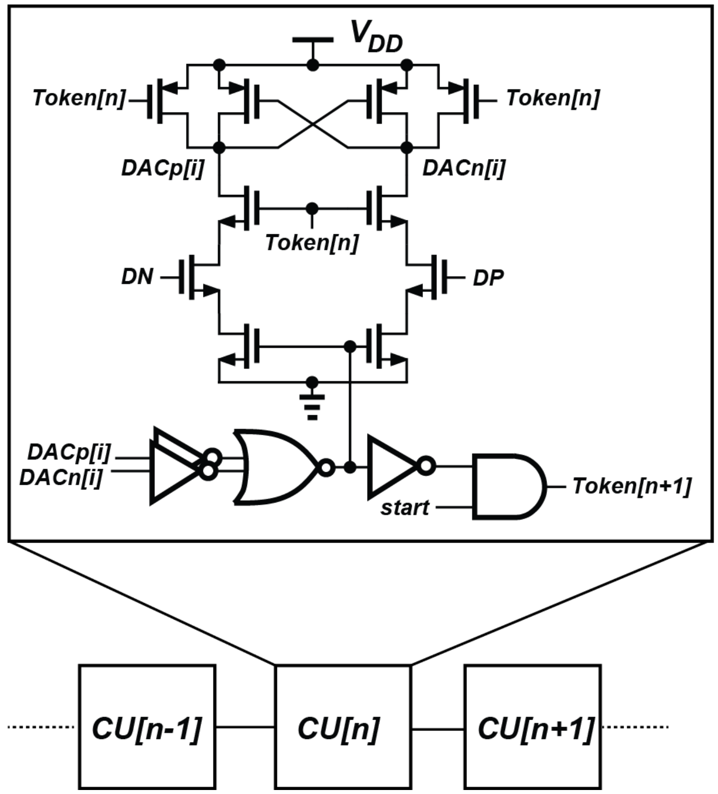


Comparator & SAR Logic

- [2] ISSCC' 15
- Low noise single phase dynamic latched comparator

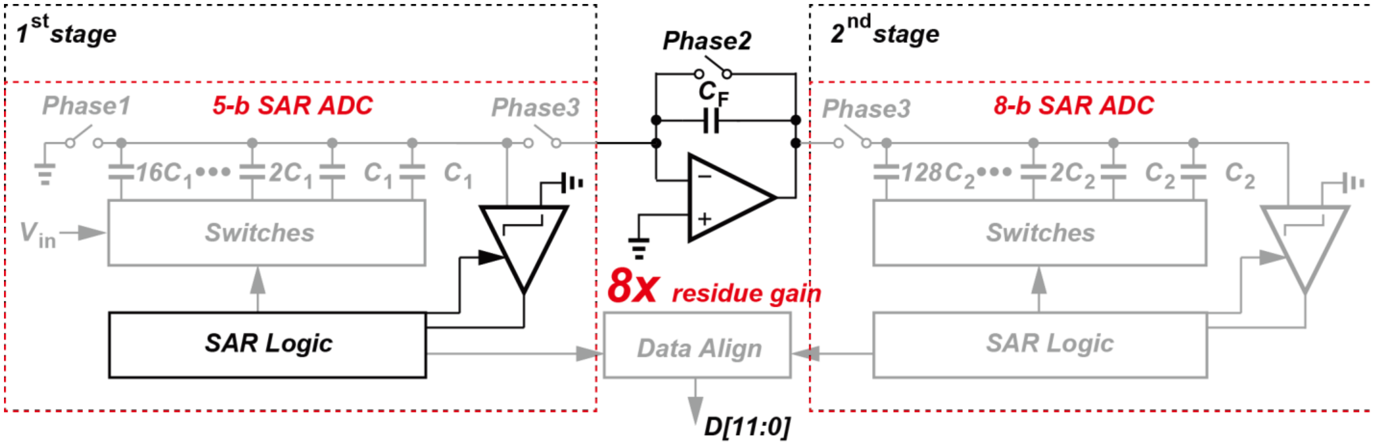


- [3] VLSI'11
- Direct switching

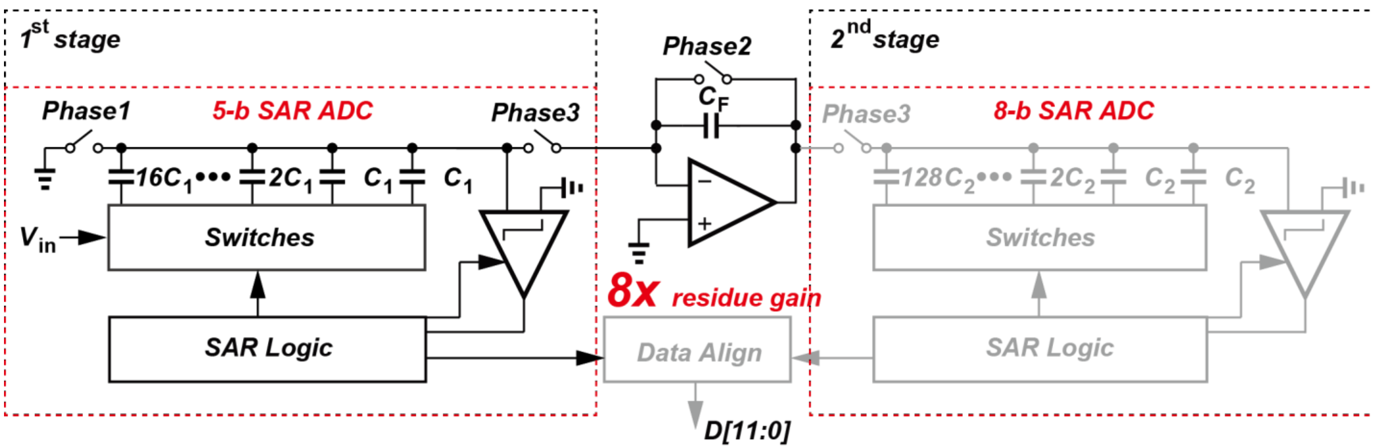


Progress

- **Things have been done:**



- **Future Plan(in the near 1 to 2 weeks):**

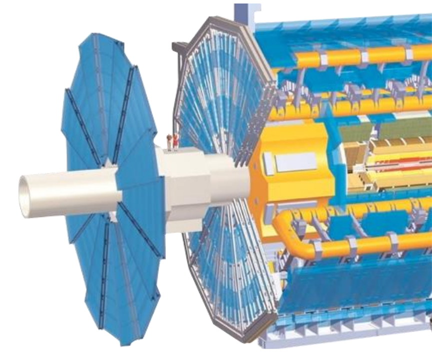


Some 12-b Prior Arts

	[4] ESSCIRC'16	[2] ISSCC'15
Architecture	Noise Shaping SAR ADC	Pipeline SAR ADC
Technology	130 nm	65 nm
DAC Calibration	No	No
Total capacitance	2.1 pF	2.048 pF
SNDR	74 dB	70.9 dB
SFDR	95 dB	84.6 dB

Reference

1. K. Bult and G. J. G. M. Geelen, “A fast-settling CMOS Op Amp for SC circuits with 90-dB dc gain,” ***IEEE J. Solid-State Circuits***, vol. 25, pp.1379–1384, Dec. 1990.
2. Y. Lim and M. P. Flynn, “A 1 mW 71.5 dB SNDR 50 MS/S 13b fully differential ring-amplifier-based SAR-assisted pipeline ADC,” ***in Proc. IEEE ISSCC. Dig. Tech. Papers***, Feb. 2015, pp. 1–3.
3. J.-H. Tsai, Y.-J. Chen, M.-H. Shen and P.-C. Huang, “A 1-V, 8b, 40MS/s, 113µW Charge-Recycling SAR ADC with a 14µW Asynchronous Controller,” ***Symp. on VLSI Circuits***, pp. 264-265, June 2011.
4. Wenjuan Guo, and Nan Sun , “A 12b-ENOB 61µW noise-shaping SAR ADC with a passive integrator ,” ***ESSCIRC,*** pp. 405-408, Oct. 2016.



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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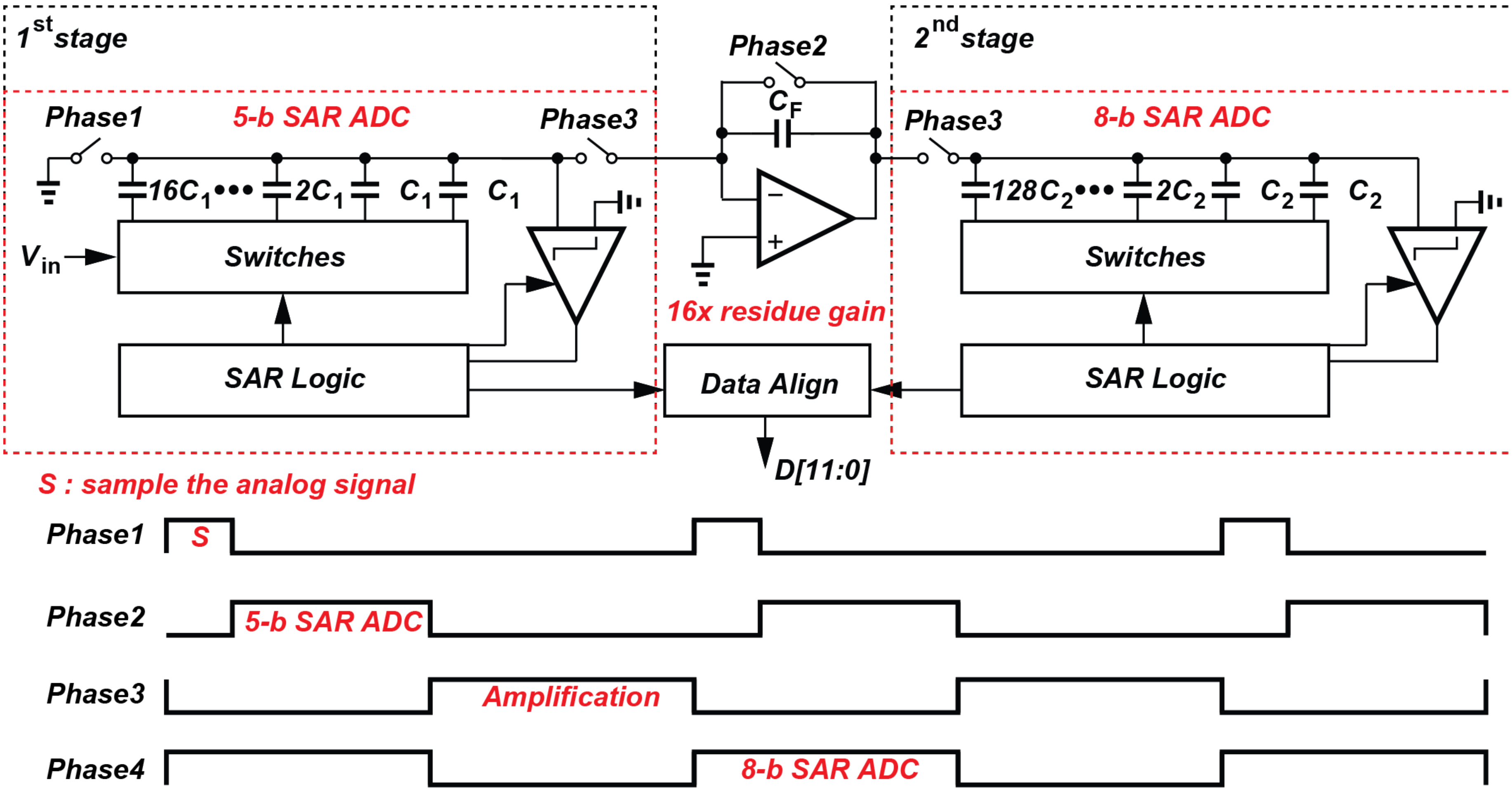
October 7, 2016

Chen-Kai Hsu

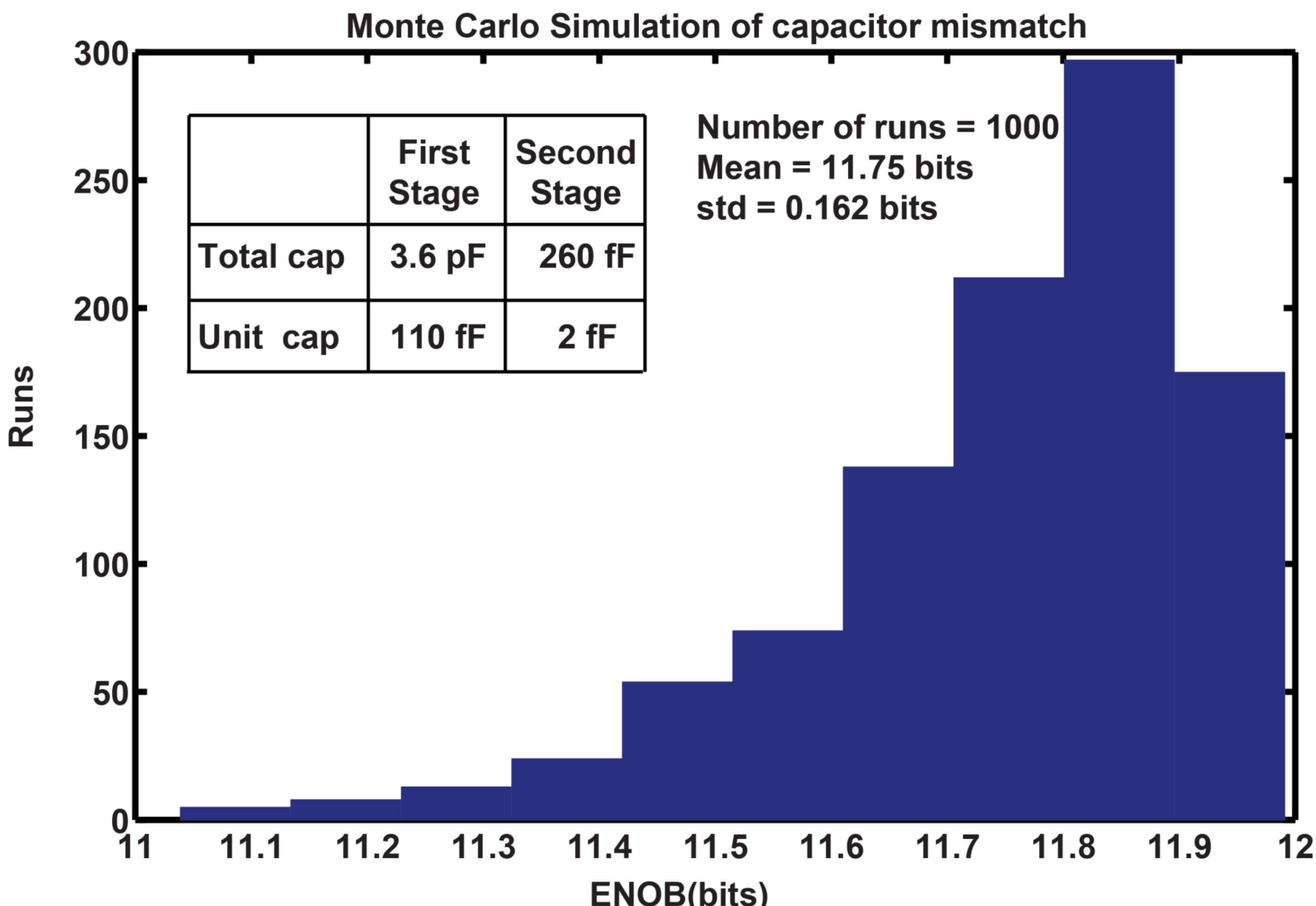
- Education
  - M.S., National Taiwan Univ., 2015
  - B.S., National Chung Cheng Univ., 2012.
- First year PhD student at UT Austin.
- My research interests include high-performance data converters, sensor interface, and mixed-signal circuits
- Process experience:
  - CMOS 0.18um / 90nm / 40nm.
- Some Research experience:
  - Low-power high-speed Pipeline ADC in 90-nm technology.
  - Low-power SAR ADC in a 0.18-um technology for smart badge.
- Publication:
  - **Chen-Kai Hsu** and Tai-Cheng Lee, "A Single-Channel 10-b 400-MS/s 8.7-mW Pipeline ADC in a 90-nm Technology." *IEEE Asian Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 233-236, Xiamen, China, Nov. 2015.

Architectural Level Plan

The ADC is a 5 + 8 bit two-step structure with 1 bit inter stage redundancy to generate a 12-bit output.



Top Level Consideration



Top Level Consideration

- **Open-loop gain consideration:**

By charge conservation, the output of a residue amplifier can be derived as:

$$V_{RES} \approx \frac{32C_1}{C_F}(VIN - \frac{1}{32}(16B_1 + 8B_2 + \cdots + B_5)V_{REF})(1 - \text{Error})$$

Where Error = $\frac{32C_1 + C_P + C_F}{AC_F}$

Therefore, in order to provide **16x** close-loop gain, we need a **78dB** open-loop gain amplifier to satisfy 8-b accuracy(1/2LSB).

- **Bandwidth consideration:**

Assuming amplifier is a single pole system, we have:

$$V_{RES} = V_{STEP}(1 - e^{-t/\tau}) \qquad \tau = \frac{1}{\omega_{3dB}}$$

At least, 1.27GHz unit-gain bandwidth is needed.

Top Level Consideration

Assuming 2 stage Miller compensated OTA:

$$Phase\ Margin = 90° - \arctan\left(\frac{g_{m1}/C_C}{g_{m2}/C_L}\right);$$

$$g_m = \frac{I_{tail}}{V_{overdrive}}$$

For Phase Margin at least greater than 65 degree,

- $I_{stage2} = I_{stage1}$ ⇨ $C_C = 2.2C_L$ (V_{eff} are the same at each stage)
- C_L =260fF(decided by monte carlo simulation). ⇨ C_C=572fF
- g_m=2*pi*1.27GHz*C_C =4.5mS
- So, $I_{stage2} = I_{stage1}$ = 0.45mA (assume $V_{overdrive}$=0.1 V)

Estimated Power

Power estimaton of this work	
Total	> 3.6 mW
Amplifier	> 1.08 mW
Ref. buffer	2 mW
others	0.9 mW

*others include
1.digital circuit
2.bootstrap switch
3.clock buffer

	This work	(1) VLSI 2010
Architecture	Pipeline SAR	Pipeline SAR
Calibration	No	No
Technology	TSMC 65 nm	65 nm
Resolution	12 bits	12 bits
Supply Voltage	1.2 V	1.3 V
Sampling Frequency	40 MHz	50 MHz
ENOB	> 11.2 bits	10.7 bits
Power	> 3.6mW	*3.5mW
Input Range(diff.)	2 Vp-p	2 Vp-p

* Power excluding reference buffer

Specification Review

	Specification	Confidence
Technology	TSMC 65 nm	OK
Supply Voltage	1.2 V	OK
Sampling Frequency	40 MHz	OK
ENOB	11.2 bits	a little tough
Power	< 20 mW	OK
Input Range	2 Vp-p	OK

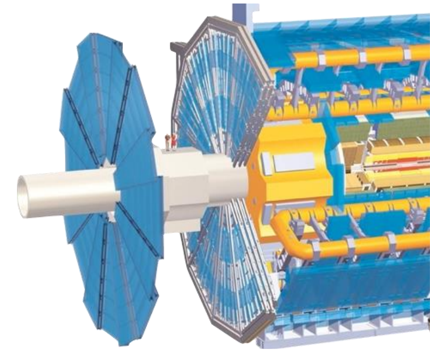
Schedule

Expected Timeline before tapeout

Oct. '16	Nov. '16	Dec. '16	Jan. '17	Feb. '17 to Apr. '17
Amplifier Design	Stage1 Design	Stage2 Design	Whole chip Optimization	Layout and post-simulation

Reference

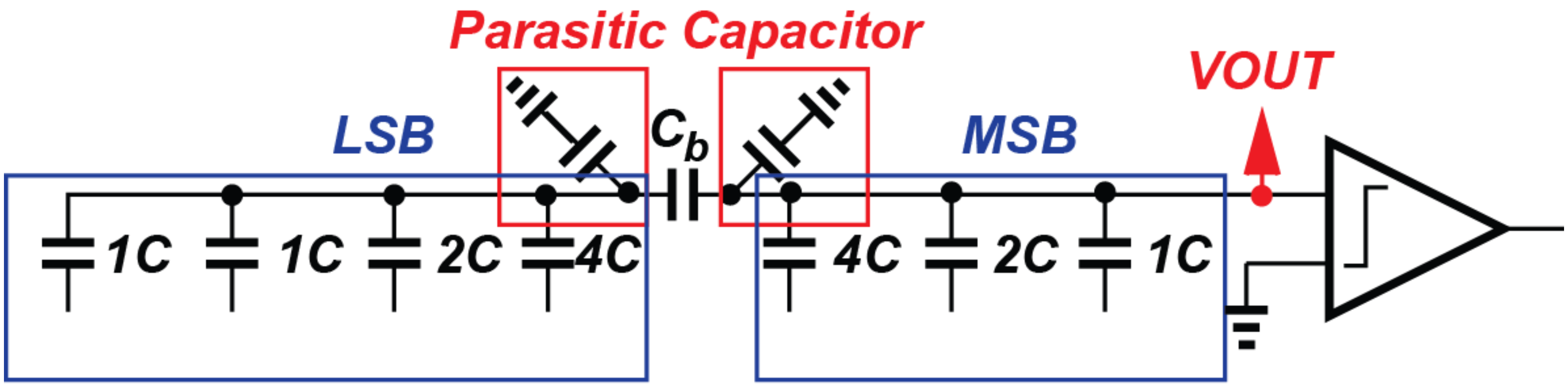
1. C. C. Lee and M. P. Flynn, “A SAR-assisted two-stage pipeline ADC,” *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 859–869, Apr. 2011.

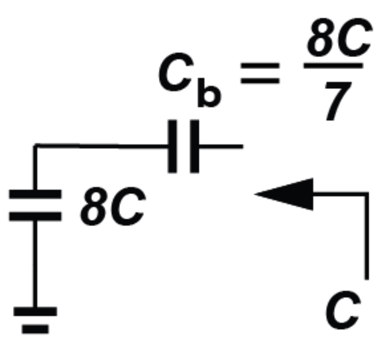


Back up slides

Solution1 for stage2

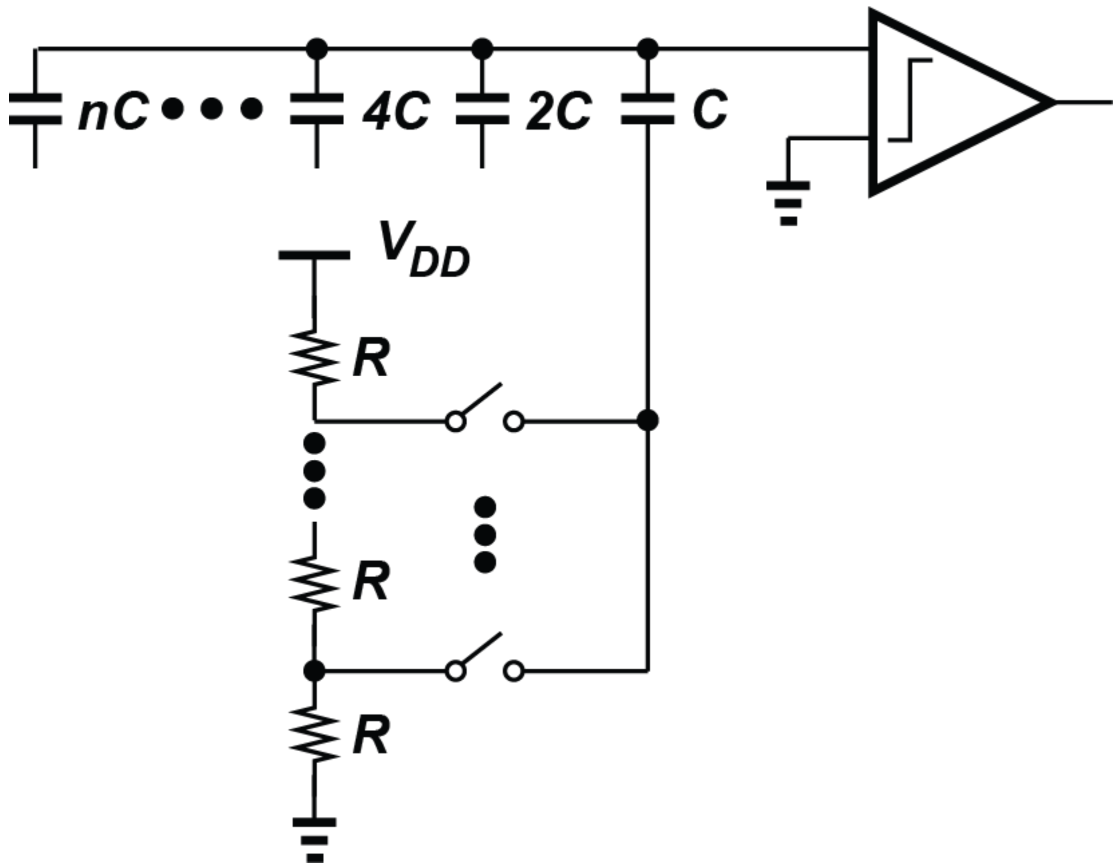
1. Bridge Capacitor Array





Solution2 for stage2

Hybrid DAC



Clock Buffer